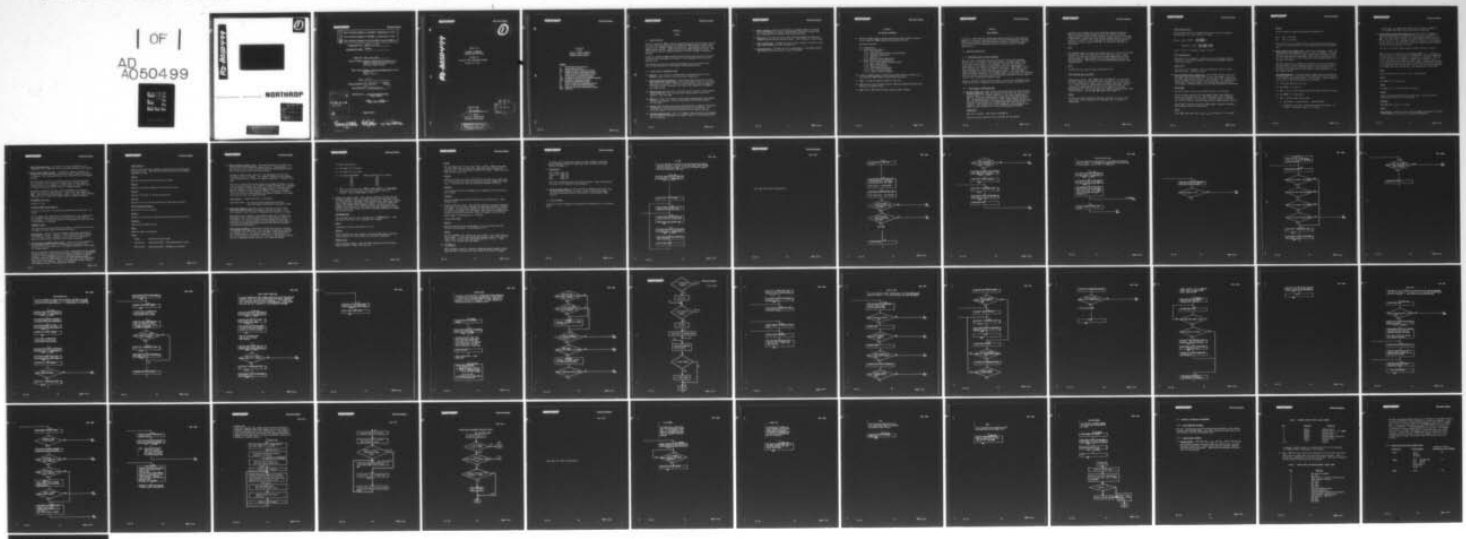
AD-A050 499 NORTHROP CORP HAWTHORNE CALIF ELECTRONICS DIV F/G 17/7
AN/BRN-7 COMPUTER PROGRAM SPECIFICATION. VOLUME 11. BUILT-IN TE--ETC(U)
OCT 73 N00039-73-C-0209
UNCLASSIFIED NORT-73-48-VOL-11 NL

1 OF 1
AD A050499



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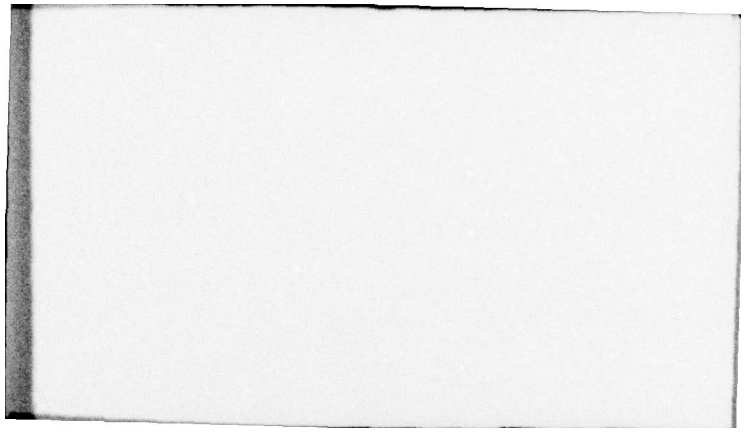

NORTHROP Electronics Division

- ☐ This submittal applies to AN/BRN-7 (Submarine Ω) only.
- ☐ This submittal applies to AN/SRN-( ) (Hydrofoil Ω) only.
- ☒ This submittal applies to both AN/BRN-7 and AN/SRN-( ).

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CDRL No: A01D, A01E, A01F

Title of CDRL: Computer Program Design Specification
Computer Subprogram Design Document
Data Base Design Document

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NORT 73-48
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FORM 6512 (2-72)

NORTHROP

Electronics Division

AD-A050499

NORT 73-48

AN/BRN-7 COMPUTER PROGRAM SPECIFICATION

Volume XI

BUILT-IN TEST SUBPROGRAM DESIGN

October 12, 1973

Approved by

G. W. Hauser
Director, Engineering
Navigation Department

Volume XI
of the
AN/BRN-7 OMEGA COMPUTER
PROGRAM SPECIFICATION

Volume	
I	Performance Specification
II	Design Specification
III	Synchronization Subprogram Design
IV	OMEGA Processing Subprogram Design
V	Tracking Filter Subprogram Design
VI	Kalman Filter Subprogram Design
VII	Propagation Prediction Subprogram Design
VIII	Navigation Subprogram Design
IX	Executive Subprogram Design
X	Control-Indicator Subprogram Design
XI	Built-in Test Subprogram Design
XII	Common Subroutines Subprogram Design
XIII	Appendix

SECTION 1

SCOPE

1.1 IDENTIFICATION

Volume I, Submarine OMEGA Computer Program Performance Specification, defines the functional requirements for the Submarine OMEGA Computer Program which is used by the AN/BRN-7 OMEGA Navigation Set. The Navigation Set and the OMEGA program together comprise the Submarine OMEGA Navigation System. The tape which defines the computer program is entitled AN/BRN-7 Navigation Program.

Volume II, Submarine OMEGA Computer Program Design Specification, allocates the functional requirements of Volume I to the computer routine and subprogram level.

This volume describes the subprogram designated as Built-in-Test which has the abbreviation TS in the program listing (Volume XIII).

1.2 BUILT-IN-TEST SUBPROGRAM TASKS

a) Receiver: The receiver is tested from the switching matrix to the computer input on each of the three basic frequencies.

b) Phase-Angle/Digital-Converter: Test signals derived from the +5 volt power source are coupled directly into the chopper circuit of the Phase-Angle/Digital-Converter. They will cause specific values to appear at the output of each converter to be read by the computer and compared with table values.

c) Phase Counter I/O: This test will exercise all functions of the up-down count accumulator buffer and the Direct Memory Access link to the computer. See next test.

d) DMA I/O: A check on the Direct Memory Access communication link between receiver and computer. Used in conjunction with the Phase Counter I/O test above.

e) Avionic I/O: An analog-to-digital conversion will be made by the Avionic I/O using the 400 Hz synchro reference signal as a reference. The resultant digital value will be verified by the computer program.

f) General Processor Test: This is a computer logic test which is designed to verify that the Arithmetic and Control section of the computer hardware is operable.

g) Memory Checksum: Verifies the contents of computer memory by summing all of the permanently stored (non-variable) contents of memory, and then comparing the sum against a pre-determined value.

h) Panel Test: Intended for use as fault isolation between the Receiver-Computer and the Control-Indicator Panel. Test indicates a faulty panel.

i) OMEGA Preamp Test: Intended for use as fault siolation of the two loop amplifiers contained in the interface box.

j) Oscillator Test: Intended for use in determining if the Omega Receiver Oscillator is operating within limits prescribed.

SECTION 2

APPLICABLE DOCUMENTS

a) Submarine OMEGA Computer Program Performance Specification (Volume I of the Submarine OMEGA Computer Program Specification).

Applicable Sections

- 3.1 Introduction
- 3.2 Functional Description
  - 3.2.1 Introduction
  - 3.2.2 Functional Description and Requirements
  - 3.2.3 Computer Input/Output
  - 3.2.4 Operation
  - 3.2.5 Detailed System Operations
- 3.3 Detailed Functional Requirements
  - 3.3.4 Bias, Scale Factor and Phase Shift
  - 3.3.5 Noise Calculations
  - 3.3.6 Phantom Calibration
  - 3.3.7 Burst Phase Measurement
  - 3.3.16 Built-in-Test Programs
  - 3.3.17 Built-in-Test Equipment

b) Submarine OMEGA Computer Program Design Specification (Volume II of the Submarine OMEGA Computer Program Specification).

c) NORT 71-41 NDC-1070 Macro Assembler, May 1971

d) NORT 68-115A, Detailed Description of NDC-1070 Computer Instructions, Revision A, February 1970.

e) NORT 69-87A, NDC-1070 Flow Chart Program, User's Manual

SECTION 3

REQUIREMENTS

In order to understand the program description contained in the following pages, it is necessary that the reader will have become familiar with the associated functional requirements found in Volume I, Performance Specification, and with the subprogram allocation found in Volume II, Design Specification.

3.1 DETAILED DESCRIPTION

3.1.1 Reference Labels to Flow Diagrams

The code used to reference the particular block in the flow diagrams, Section 3.2, is as follows: The first number is the page number found in the upper right corner of the diagrams. This will be followed by a slash sign (/) to separate the page number from the block designator. The designator will either be a mnemonic label (e.g., TEST SYNC), a local label indicated by a dollar sign ($), or an integer. The two types of labels reference the particular information block, on the given page, to which the label is attached. The integer number, n, means that the referenced block is the n^{th} block from the top of the page; p8/3 would refer to page 8 and the third information designator down.

Finally, the label p1/$2+3 refers to page 1, and the 3rd information block after the label $2. Similarly, p2/7,8,9 refers to page 2 and blocks 7-9.

3.1.2 Description of Flow Diagrams

a) RF Test (Pages 1-4): Test signals derived directly from the Precision Frequency Generator (PFG) are coupled directly into the input of each Switching Matrix in a manner identical to the normal (operational) signals. These test signals have a known phase relationship with the PFG. These signals are switched as inputs, under computer control, into the Switching Matrix; the signals are passed through the remaining portions of the receiver in a normal manner and then read by the computer. The incoming data (in the computer) is then compared with known data and verified to be within predetermined tolerances.

P1/RF Test:

Set $\Delta t\,\Omega$ = 1 second. Next Ωtask to RF TEST $1.

This will permit test data to be collected for one second.

Included as an integral part of the Precision Frequency Generator (PFG) is a Digital Phase Comparator which will detect an out-of-synchronization condition of the frequency divider network of the PFG. A BITE signal is generated by the computer program when an out-of-sync condition is detected. The computer will sense this condition and generate a re-sync signal to the PFG. At this point the PFG is initialized.

P1/2

The program selects the test +90° signals for 10.2, 13.6 and 11-1/3 kHz frequencies. Each is a square wave with a 50% duty cycle. Each signal is derived from a flip-flop in the PFG, phase shifted by 90° and attenuated to approximately -65 db prior to insertion into the Switching Matrix. This signal tests the (COSINE) phase-shifted input characteristics.

P1/3:

On DMA words 20_{16} 21_{16} and 22_{16} select R(x) TQ =1.

P1/$1 Through Loop to p1/$11:

Repetition of above. Next OMEGA task is RF TEST $2. At this point the test signals are switched into the receiver for 10.2, 13.6 and 11-1/3 KHz frequencies. Again, each is a square wave with a 50% duty cycle. Each signal is derived from a flip-flop in the PFG, and is attenuated to approximately -65 db prior to insertion into the Switching Matrix. This signal tests the (SINE) non-phase-shifted input characteristics. For the same DMA words select R(x)T = 1.

P3/$2:

The data for these frequencies has been collected. If this is Pre-flight Test all six inputs will be evaluated and a 3 counter is established.

P3/$4 through P3/5:

For Preflight Test the following will be done for each frequency sequentially; 10.2, 13.6, then 11-1/3 KHz.

Obtain $\alpha(T) = TAN^{-1} \frac{SIN\ (TEST)}{COS\ (TEST)}$

$$\alpha(T+90°) = TAN^{-1} \frac{SIN\ (TEST + 90°)}{COS\ (TEST + 90°)}$$

Test: Is $67.5° < \alpha(T+90°) - \alpha(T) < 112.5°$?

P3/6 through P4/3:

Test pass on one frequency. Either select test inputs on another frequency or set Phase-to-Digital test as the next OMEGA task and $\Delta t\Omega = 0.02$ second.

P4/$5, $5+2:

Test fail on one frequency. Turn on malfunction lamp on control indicator panel. Continue RF test.

b) Phase-to-Digital Test (Pages 5-8): Test signals derived from the +5 volt power source are coupled directly into the chopper circuit of the Phase Angle/Digital Converter. These signals will cause specific values to appear at the output of each converter. The computer then reads these values and compares them against predetermined values to determine a GO/NO-GO condition of the Phase Angle/Digital Converter.

P5/PD TEST:

Set next Ω-task as this one at p5/$1, and $\Delta t\Omega$ = 1.0 second.

The test signal consists of using Computer Logic Level Signal an input to the chopper circuit. The test signal is then processed in a normal manner by the converter. The test signal is switched into all six converter circuits concurrently, under computer control.

Signal PDT = Select test input to Phase Angle to Digital Converter. (All channels selected concurrently).

P5/2:

Clear DMA input words 20_{16}, 21_{16}, 22_{16}, and return in 1.0 second.

P6/$10:

On each frequency sequentially perform following test

Test: $516 < \cos < 1600$

and $516 < \sin < 1600$?

For test fail on any frequency turn on system malfunction indicator on Control-Indicator Panel. For test pass continue to Phase Counter test.

c) Phase Counter Test (pages 9,10): This test is designed to check the communication link between the Receiver and the Computer. The test exercises all the functions of the up-down count accumulator buffer and the Direct Memory Access (DMA). When used in conjunction with the I/O - DMA Test, the entire functional link between Receiver and Computer is verified.

The test consists of a seventh (in addition to the six sine/cosine up-down signals) signal signifying count up or count down, which is provided as an input to the Phase Counter. This seventh word is treated in the same manner as the other six from this point on into the computer memory.

Test Mechanization: A constant count up-down signal is provided as an input signal to the phase counter by applying a flip-flop output as an input to the phase counter. A true (logic 1) signal signifies count up and a false signal signifies count down.

1) Initialize DMA word 16 to zero

2) Set PHTST = 1 (count up)

3) Wait 1 second, then read and test that input exceeds 400 counts.

4) Set PHTST = 0 (count down)

5) Wait 1 second, then read and test.

   a. Test Select: Test selected precruise test.

   b. Tolerance: Up count - down counts must be less than ± 15 counts. Count per 5 msec = 15, ±1 count.

Notice that the Phase Counter Test does not setup the DMA test as an OMEGA task; DMA test follows normal sequencing.

d) Direct Memory Access Test (Pages 11, 12): This test is designed to check the communication link between the receiver and computer. A memory cell location is brought out to the Transfer Buffer via the DMA. The adder control causes the Transfer Buffer to be incremented by the value -1. This incremented value is returned to the original memory cell again via the D or A, where the computer verifies that the cell has been incremented correctly.

The test is initiated under computer program control at turn-on.

When the test is selected by the computer (RDMAT = 1), a constant -1 value is added to the contents of the DMA word. This is accomplished by switching in a +5 vdc signal at the input to the adder. The test word is brought out from memory, via DMA, and is added to the -1 value, then returned to memory via DMA. This is repeated seven times in 5 milliseconds, since the logic of the adder under normal operation is to add the contents of the seven words in the circulating register to the DMA words 10_{16} through 16_{16}. The sequencing is as follows:

P11/1:

Next Ω-task as this one at $1, $\Delta t\,\Omega$ = 0.005 second.

P11/2:

Set RDMAT true in word 23_{16}.

P11/3:

Set word 17_{16} = 0 to start data collection.

P11/$1:

After 5 milliseconds sequencing returns here. Set next Ω-task = synchronization and $\Delta t\,\Omega$ = 0.2 second.

P11/$1+1:

Test DMA word 17_{16} for -7 counts

P11/6:

Test Failure: Failure of test value to compare constitutes a failure in the Computer I/O section of the Receiver-Computer.

Test Timing and Delay: Test takes two 5 msec interrupts to be completed. Test is selected on the first and verified on the second.

e) Avionics Test (Pages 13-15): A conversion, analog-to-digital, is made by the Avionic I/O using the 400 Hz synchro reference signal as a reference. The resultant digital value is verified by the computer program.

The test signal consists of attenuating the 26 VAC, 400 Hz signal, and treating this as a normal ac voltage input. Under computer program control, this channel is converted and the resultant value is compared against prestored values in computer memory.

Upon entry in Avionic I/O test, routine addresses the reference channel conversion storage location. (Data is put into memory via DMA). Upon conversion complete, the value is read and compared against prestored value. Failure to compare results in NO-GO situation.

P13/ADTEST, $1, $1+1:

Entrance to test.

P13/AD IO TEST through Page 15:

A failure in any pass is a test-word reading which exceeds 486 ± 24 counts.

The 12 counter will keep track of the failures in a set. After a set of 12 passes another memory word will keep track of the number of failed passes. If three have failed in the sequence of five sets then a test failure is indicated.

P15/$3+2 to end.

The excitation A and excitation B is checked. If present then return. If either is faulty then post failure and return.

Test Failure: Failure to convert properly indicates a malfunction of Avionic I/O section. However, if the 26 VAC reference is absent, test indicates failure. Operator is then required to determine if failure is due to faulty Avionic I/O or loss of reference.

f) 1070 A/C Test (GP TEST) (Pages 16-18): This test is also referred to as the Computer Logic Test. It is designed to verify that the arithmetic and control section of the computer hardware is functioning in a normal manner.

The test consists of execution of the basic instructions of the computer being executed and being checked for proper bit patterns in appropriate registers. Upon completion of this a "sample problem" is executed, primarily using the ARCTAN routine of the normal program storage. This routine was selected because it uses about 90% of the instruction repertoire of the computer. The test is mechanized entirely within the computer program of the operational routines.

P16/GP TEST, 2:

Exercise fetch and fetch immediate instructions to load registers with known values. Exercise the addition instruction and compare immediate to check.

P16/3,4:

Exercise the subtraction instruction and check.

P16/5,6:

Exercise the compare immediate instruction and check.

P16/7,8:

Exercise the branch on overflow instruction.

P17/1,2:

Exercise the clear and add instruction using index registers.

P17/$1 through P17/$1+4:

Exit loop in case of failure.

P17/$2:

Exercise roll function of push-down stack with prime instruction.

P17/$2,3:

Exercise arc tangent routine.

P18/1:

Exercise square root routine.

NOTES:

Timing	Executed once per second.
Test Select	Operational Mode - Entry periodically (1/sec)
Test Failure	Operational Mode - SYS MALF is turned ON

g) Memory Checksum (Pages 19-20): The memory checksum is provided as a test to verify the contents of computer memory. Operationally, it is performed at turn-on (after Preflight Test) and as background in the main program during slack processing periods.

The Memory Checksum Test sums all of the permanently stored (non-variable) contents of memory. The computer compares the sum against a predetermined value; failure to compare constitutes a failure of the test.

This test is mechanized entirely within the computer software. At the time of program assembly, the assembler program generates the "checksum" for that program assembly and places this value in a storage location. When the program is loaded into the OMEGA computer, this checksum shall be constant for the program as loaded. If memory is altered in any way from the loaded program, the checksum constant is no longer valid and the test will indicate failure.

Test Failure: If NO-GO condition is indicated:

Operational Mode - Set flag and System Malfunction Indicator. (Receiver-Computer Malfunction indicator set ON.)

h) Panel Test (Pages 21-23): This test is intended for use as fault isolation between the Receiver-Computer and the C-I panel. It is not intended to fault isolate to subassemblies within the C-I panel.

Upon demand of the operator, the computer causes the indicators and segmented displays (lamp filaments) to be turned ON for a period of 10 seconds. This test overrides any other display data and upon completion of the 10-second period the operator must verify that all indicators and segmented displays are ON in the pattern described in the Pre-Cruise Procedure.

Test Timing and Delay: The momentary switch data from the C-I panel is available in the DMA table. An interrupt is generated, signaling the computer that a switch has been activated. Upon recognition of the interrupt signal, the program causes all the indicators to be set in the pattern for a period of 10 seconds. (See Volume X, Control Indicator Subprogram Design, Section 3.3.4, Panel Interrupt).

C-I Panel Test Pattern

1) All lamps on (2 seconds)

2) All lamps off (2 seconds)

3) Left Legend MIN/KNOTS Right Legend R/L (on 1 second)

N/S	E/W
H/G	H/G
F/E	F/E
D/C	D/C
B/A	B/A

4) Panel in quiescent state; INSERT, CLEAR DISPLAY on, HOLD/NORMAL restored to previous state, all status lamps restored to previous state and MALF lamp is left off.

i) Preamp test (pages 24-25): Test signals, derived from the Precision Frequency Generator (PFG) are coupled directly into the input of the two loop amplifiers contained in the Interface Box. These test signals have a known phase relationship with respect to the PFG. These test signals are switched under computer control, into the system; the computer then reads the receiver phase angle and compares this value against a pre-stored value. Any out-of-tolerance condition is defined as a system failure.

P24/Preamp Test

Set next task time to 1 sec. and next task to PREAMP_TEST $1. This will permit test data to be collected for 1 second.

P24/2

Initialize the PFG as described in 3.1.2a.

P24/3,4

After resetting all test signals in the Test Signal Output word the program selects the loop A signal for the three frequencies.

P24/5 at $11.

Output selected signals, clear the data collection cells and start data collection. After 1 sec go to $1.

P24/$1

Set next Omega task = $2 to occur after 1 second. Compute the angle for loop A and save for later use. Now select loop B signal and branch to $11. This initializes antennas for loop B. Return from $11 this time will be to $2.

P/25,$2

Compute the angle for loop B and subtract the saved loop A angle from it. Test the absolute value of the result with the preamp test angle limit. If greater the test has failed and proceed to P/25$12.

P/25,$21

If test passed set the next Omega task to begin the RF test and exit this routine.

P/25,$12

Turn on the MALF lamp and past failure bits in failure word. Then proceed to $21.

j) Frequency Stability Test: The receiver oscillator frequency variation with respect to the signal frequency provides the oscillator effective time drift. The short term stability of the oscillator is specified as .001 Hz rms averaged for one second. This value of frequency drift provides an effective time drift ($T_0^{\cdot}$) with respect to the 10.2 kHz Omega signal of approximately 0.1 sec/sec.

P26/OSC TEST ENTRY

P26/1,2

Has synchronization been established? If no, skip this test and return to main program. If yes proceed to $1.

P26/$1

Has the VARIANCE of $T_0^{\cdot}$ reached its limit value? If no, then return to main program. If yes, then compare the absolute value of $T_0^{\cdot}$ with its limit value. If less then test passed and exit. If no, test failed. Post failure bits and return.

k) P32/OPER_P_C

The programmer controller routine is entered once per second via the SLOW routines in the executive (see Volume IX, Executive Programs).

It causes a two hexidecimal display on the programmer controller which represents either all tests pass (00), or one test failure (E2-F4) see Table 3.

l) Subroutines:

Fail Common (Page 28)
Signal Pin (Page 29)
Fail (Page 30)
Mark (Page 31)

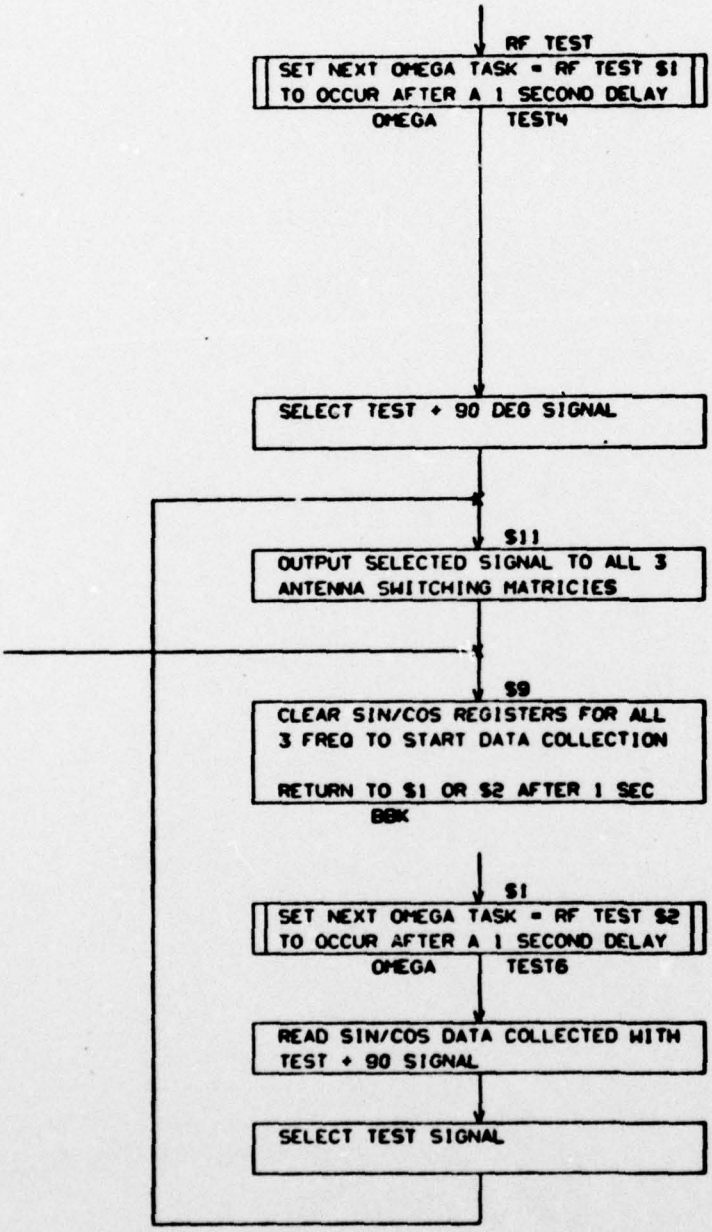
These are subroutines used by the Test routines. Their descriptions are given on the respective flow diagrams.

m) Receiver Error (Page 32): This routine is entered whenever the bias or scale factors are out of limits. Refer to Volume IV, Omega Processing Subprogram Design, description of flow diagram, pages 8 and 9.

3.2 FLOW DIAGRAMS

The Built-in-Test Subprogram flow diagrams are presented on the following pages.

• RF TEST
•
• THIS TEST COMMANDS TEST SIGNALS IN EACH RF STRIP AND THEN CHECKS
• THE RESULTING INPUT. THIS TEST IS THE FIRST OMEGA TASK AFTER TURN
• ON AND IS EXECUTED ONLY ONCE. IT CYCLES TO THE PHASE TO DIGITAL
• TEST AFTER COMPLETION IF PREFLIGHT.



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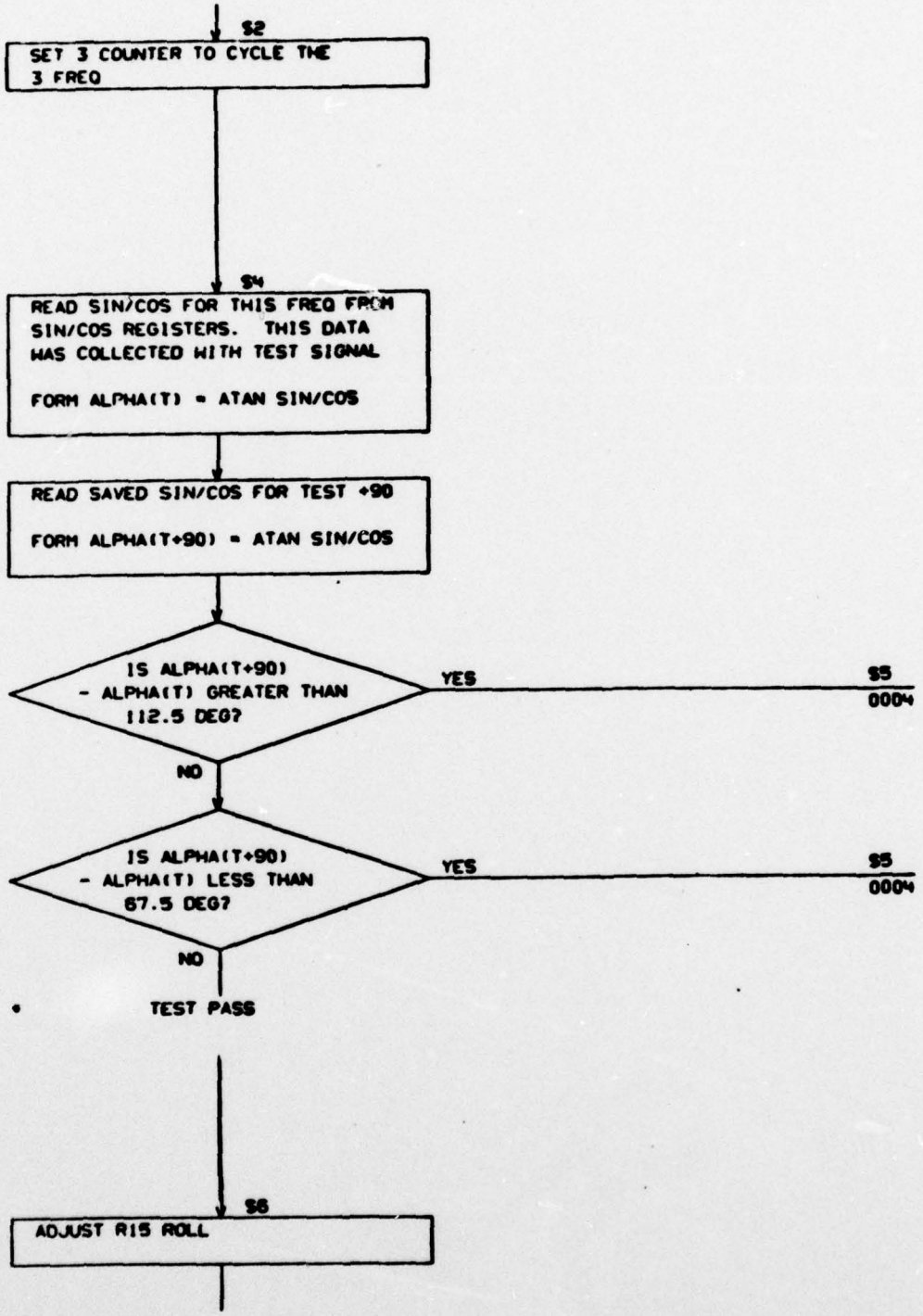
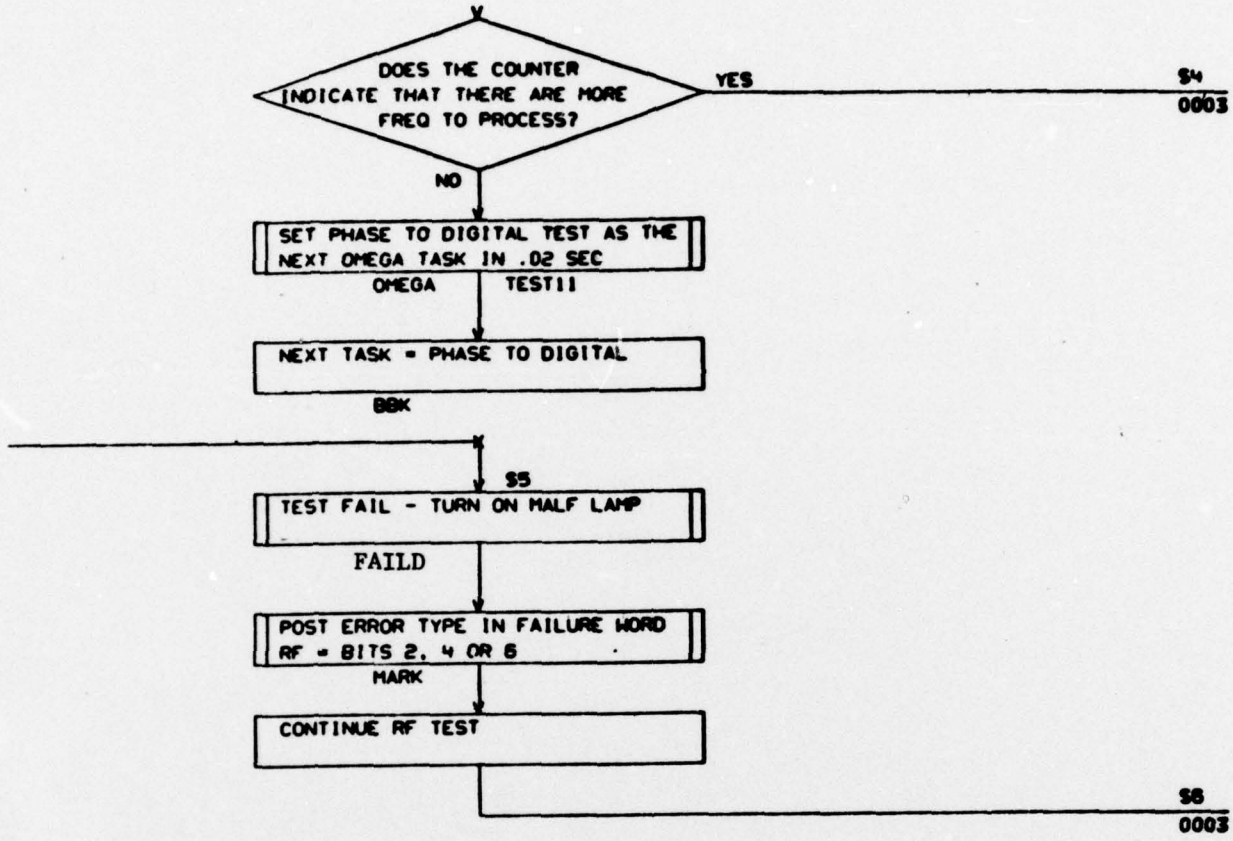
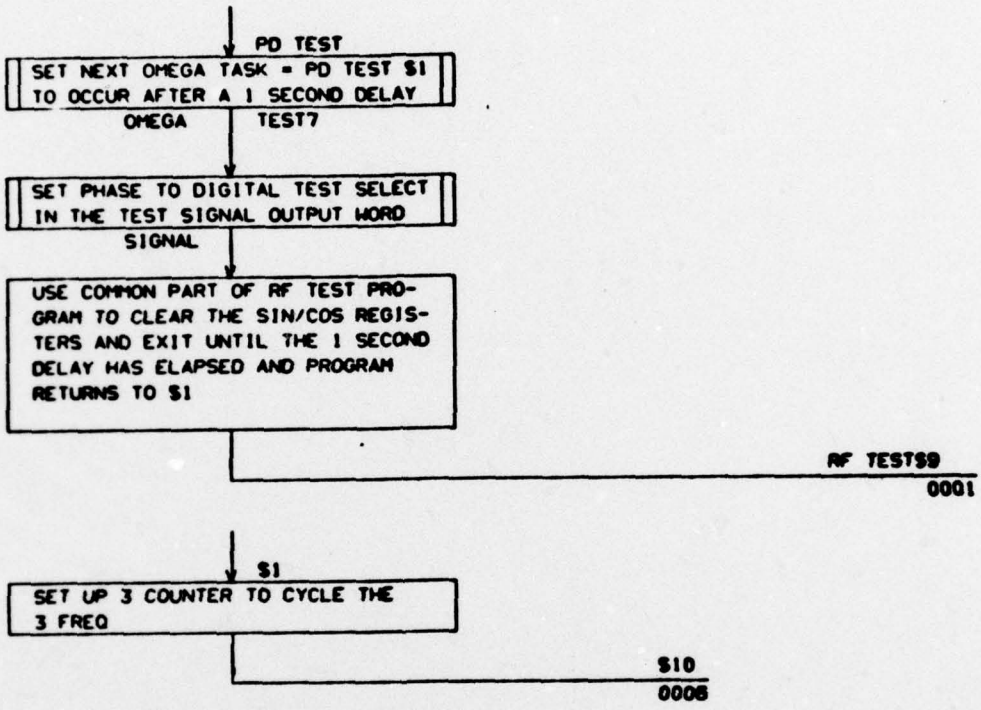
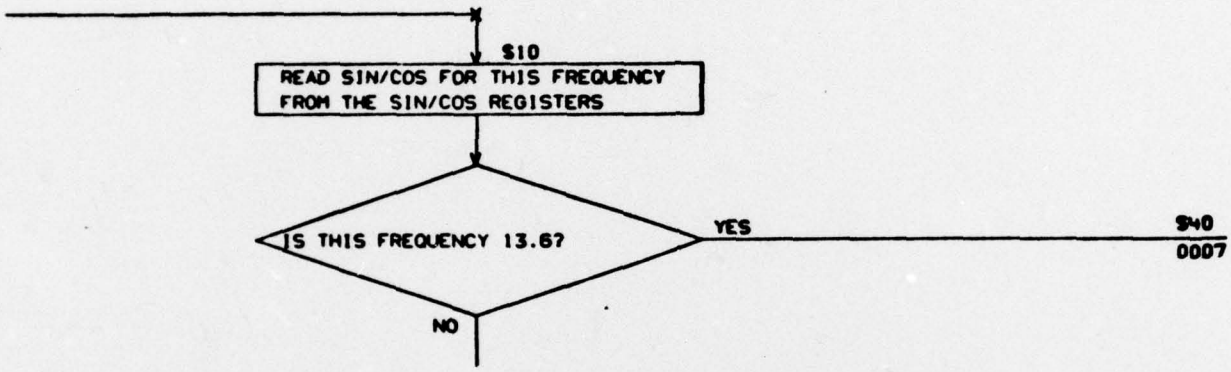
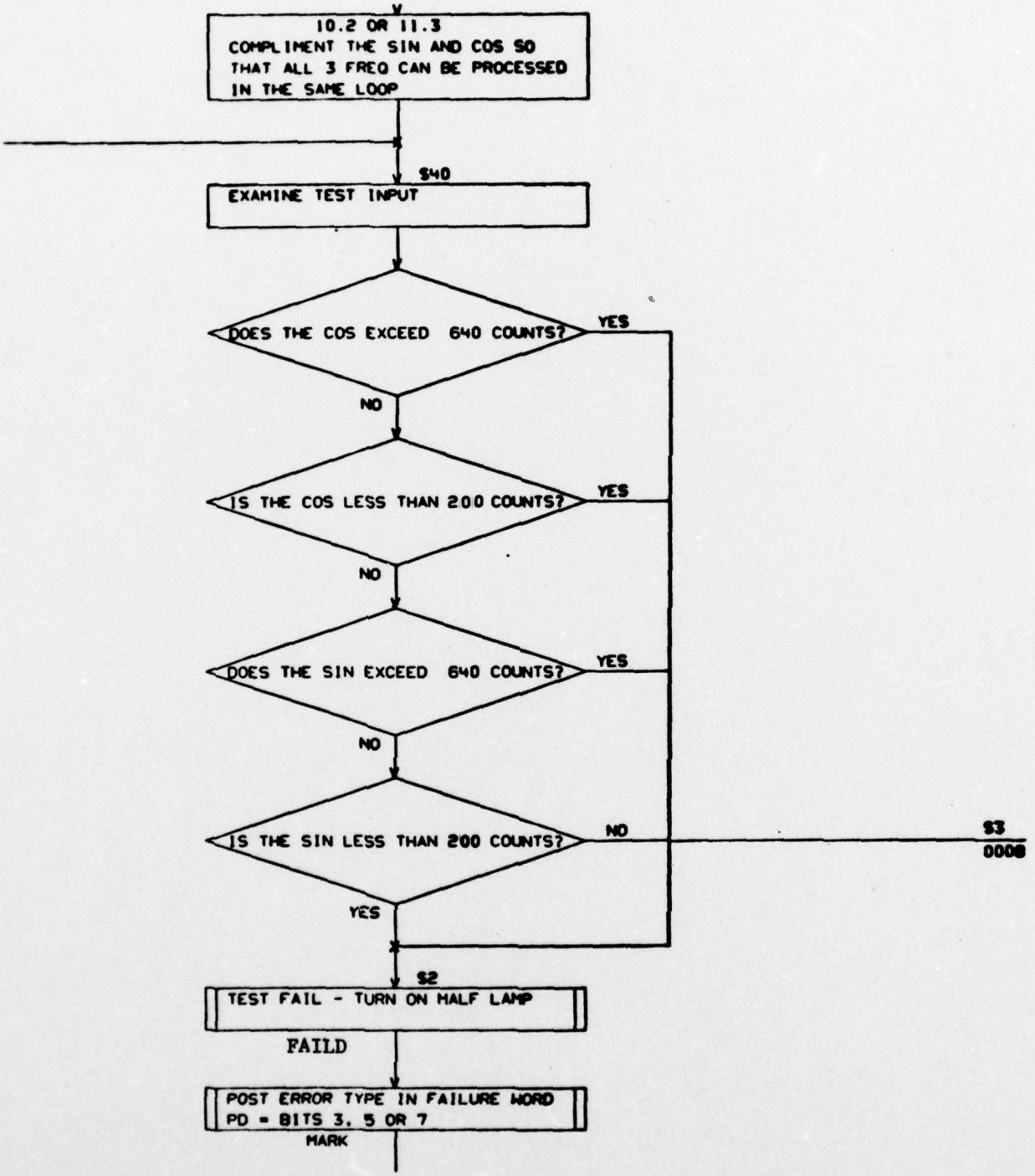

S2
SET 3 COUNTER TO CYCLE THE 3 FREQ
S4
READ SIN/COS FOR THIS FREQ FROM SIN/COS REGISTERS. THIS DATA WAS COLLECTED WITH TEST SIGNAL
FORM ALPHA(T) = ATAN SIN/COS
READ SAVED SIN/COS FOR TEST +90
FORM ALPHA(T+90) = ATAN SIN/COS
IS ALPHA(T+90) - ALPHA(T) GREATER THAN 112.5 DEG?
YES
S5
0004
NO
IS ALPHA(T+90) - ALPHA(T) LESS THAN 67.5 DEG?
YES
S5
0004
NO
TEST PASS
S6
ADJUST R15 ROLL

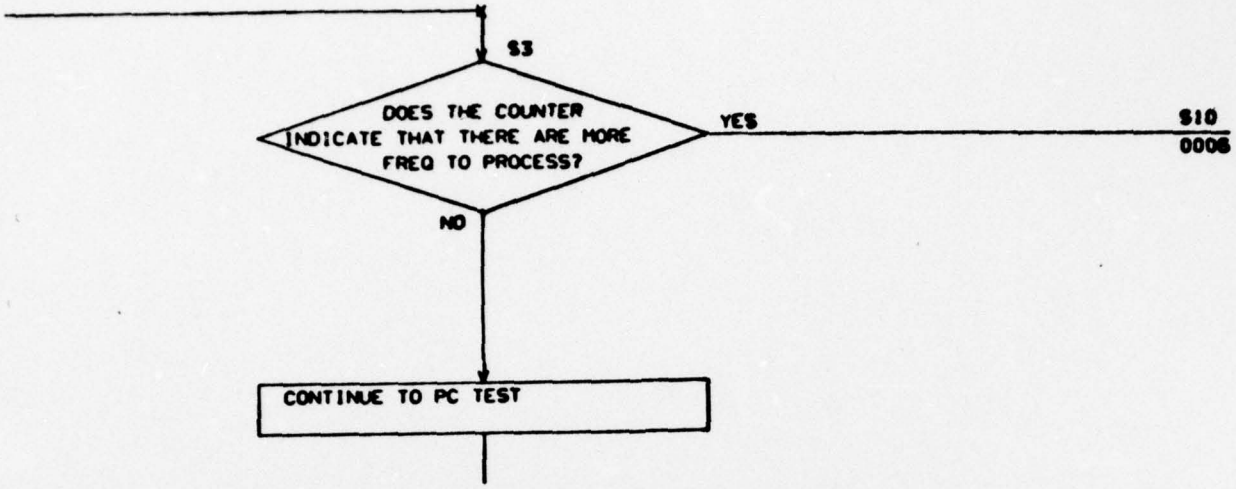

DOES THE COUNTER INDICATE THAT THERE ARE MORE FREQ TO PROCESS?
YES
$4
0003
NO
SET PHASE TO DIGITAL TEST AS THE NEXT OMEGA TASK IN .02 SEC
OMEGA
TEST11
NEXT TASK = PHASE TO DIGITAL
BBK
$5
TEST FAIL - TURN ON MALF LAMP
FAILD
POST ERROR TYPE IN FAILURE WORD
RF = BITS 2, 4 OR 6
MARK
CONTINUE RF TEST
$6
0003

• PHASE TO DIGITAL TEST
•
• THIS TEST COMMANDS THE CONVERSION OF A FIXED SIGNAL AND CHECKS THE
• RESULTING INPUT. IT IS AN OMEGA TASK EXECUTED AFTER THE RF TEST AND
• IT THEN SEQUENCES TO THE PC TEST IF IN PREFLIGHT.
•

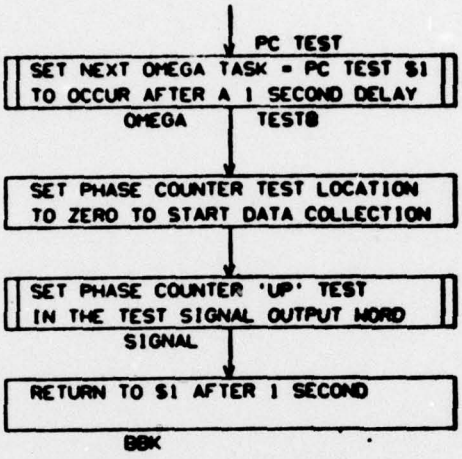



$10
READ SIN/COS FOR THIS FREQUENCY
FROM THE SIN/COS REGISTERS
IS THIS FREQUENCY 13.6?
YES
$40
0007
NO

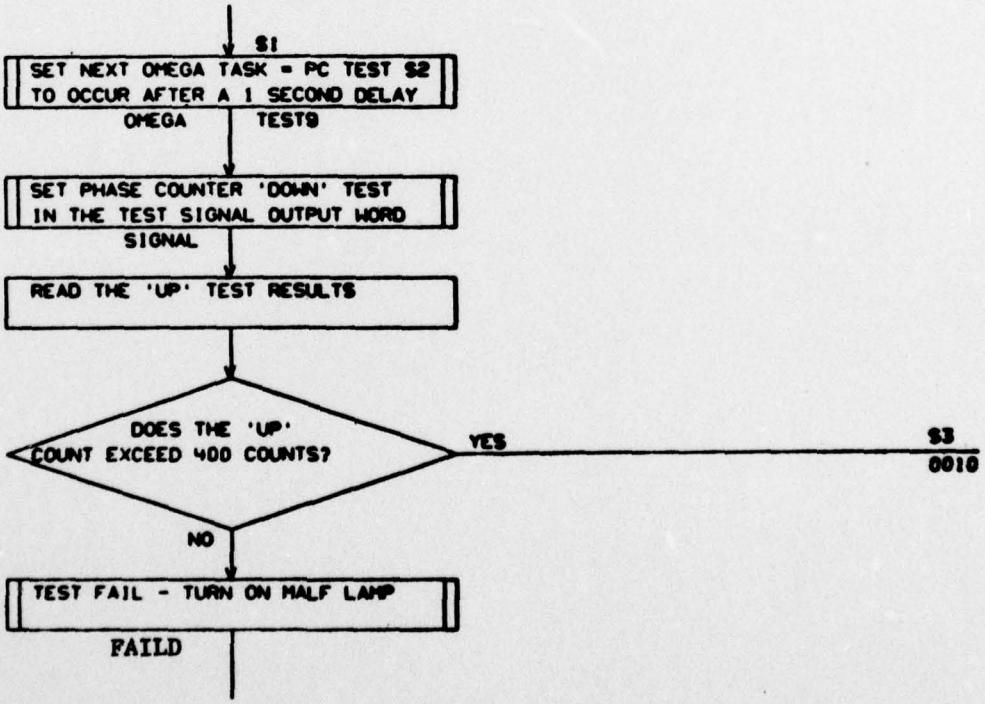

10.2 OR 11.3
COMPLIMENT THE SIN AND COS SO
THAT ALL 3 FREQ CAN BE PROCESSED
IN THE SAME LOOP
$40
EXAMINE TEST INPUT
DOES THE COS EXCEED 640 COUNTS?
YES
NO
IS THE COS LESS THAN 200 COUNTS?
YES
NO
DOES THE SIN EXCEED 640 COUNTS?
YES
NO
IS THE SIN LESS THAN 200 COUNTS?
NO
$3
0008
YES
$2
TEST FAIL - TURN ON MALF LAMP
FAILD
POST ERROR TYPE IN FAILURE WORD
PD = BITS 3, 5 OR 7
MARK

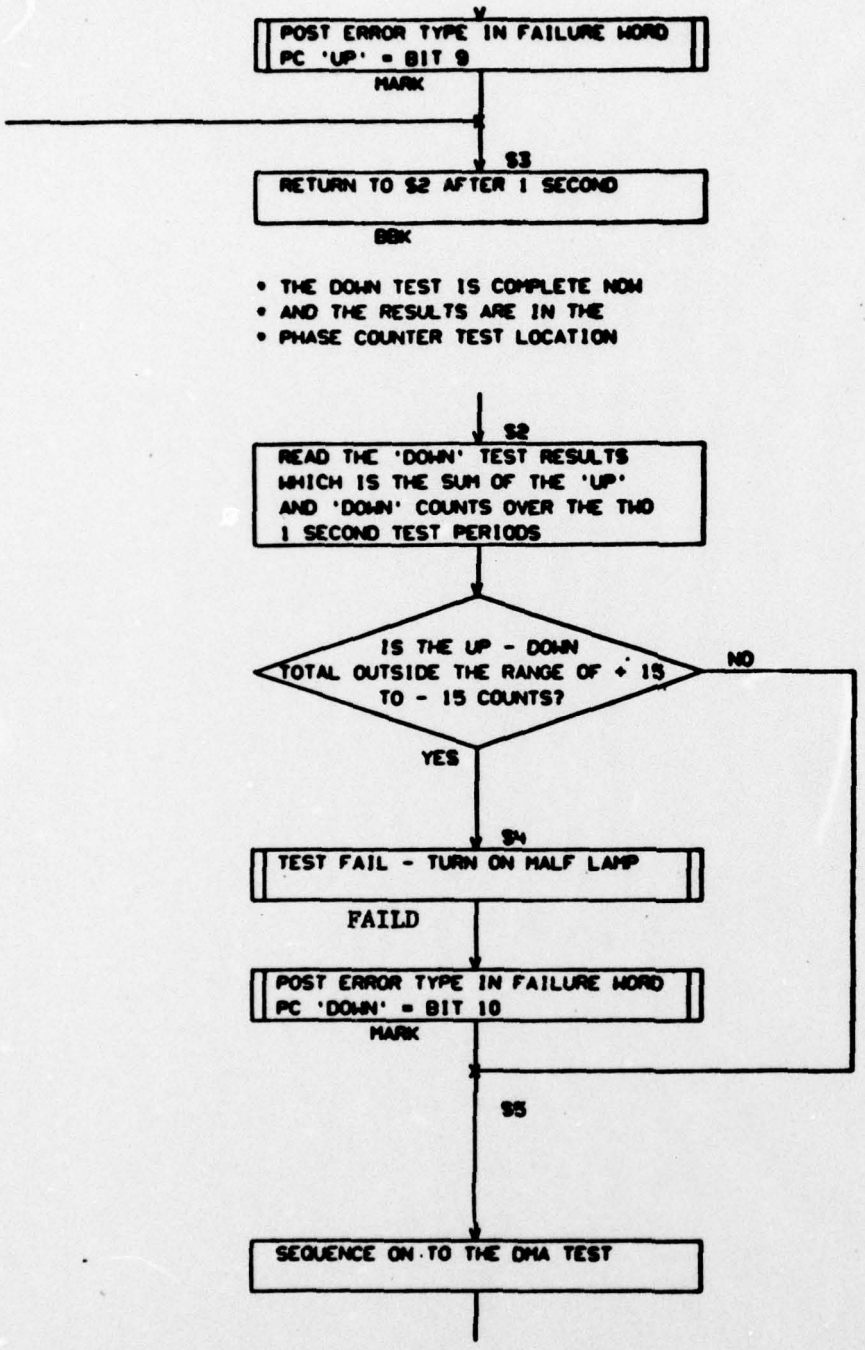

$3
DOES THE COUNTER INDICATE THAT THERE ARE MORE FREQ TO PROCESS?
YES
$10
0006
NO
CONTINUE TO PC TEST

```
•                    PHASE COUNTER TEST
•
• THIS TEST COMMANDS THE PHASE COUNTER TO COUNT UP AND DOWN IN THE TEST
• LOCATION AND CHECKS THE RESULT.  IT IS AN OMEGA TASK THAT IS EXECUTED
• AFTER THE PD TEST DURING PREFLIGHT.  IT THEN SEQUENCES TO THE DMA TEST
•
```



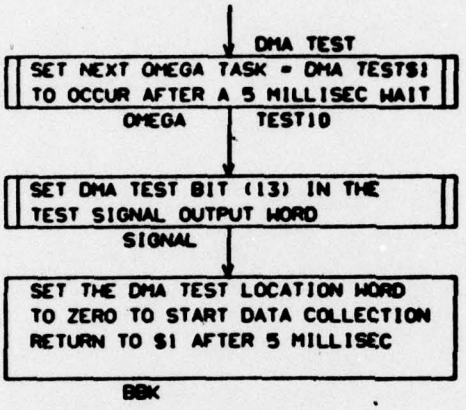

```
• THE UP TEST IS COMPLETE NOW
• AND THE RESULTS ARE IN THE
• PHASE COUNTER TEST LOCATION
```



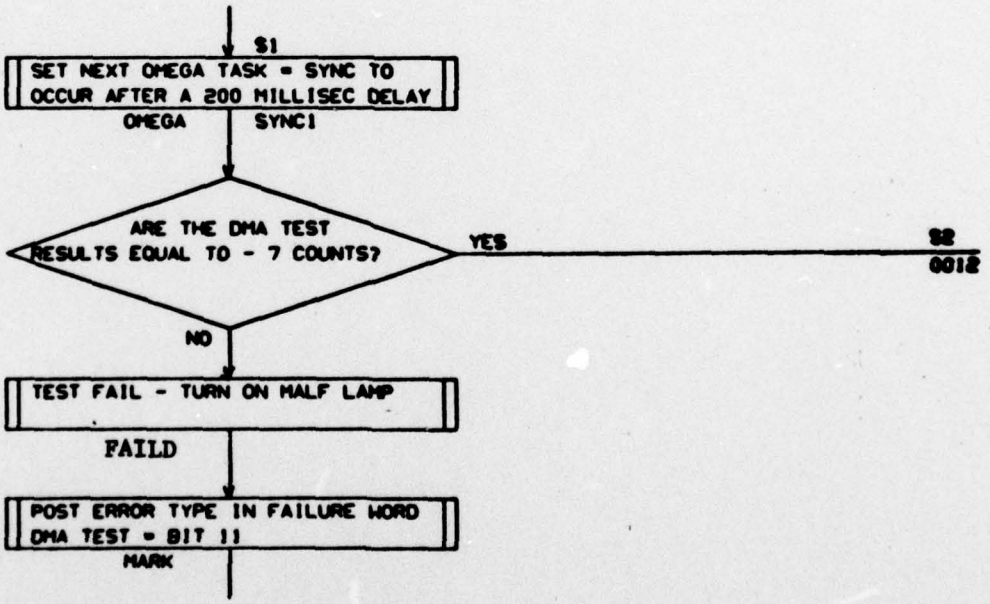

POST ERROR TYPE IN FAILURE WORD
PC 'UP' = BIT 9
MARK
S3
RETURN TO S2 AFTER 1 SECOND
BBK
• THE DOWN TEST IS COMPLETE NOW
• AND THE RESULTS ARE IN THE
• PHASE COUNTER TEST LOCATION
S2
READ THE 'DOWN' TEST RESULTS WHICH IS THE SUM OF THE 'UP' AND 'DOWN' COUNTS OVER THE TWO 1 SECOND TEST PERIODS
IS THE UP - DOWN TOTAL OUTSIDE THE RANGE OF + 15 TO - 15 COUNTS?
NO
YES
S4
TEST FAIL - TURN ON MALF LAMP
FAILD
POST ERROR TYPE IN FAILURE WORD
PC 'DOWN' = BIT 10
MARK
S5
SEQUENCE ON TO THE DMA TEST

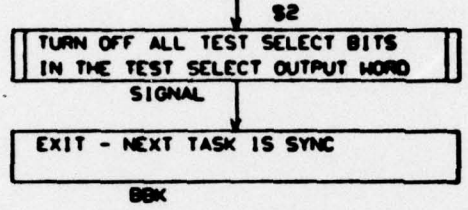
DIRECT MEMORY ACCESS TEST

THIS TEST COMMANDS THE DIRECT MEMORY ACCESS TO GO TO THE TEST MODE AND DECREMENT THE DMA TEST LOCATION WORD FOR EACH DMA INPUT (A TOTAL OF 7 EVERY 5 MILLISEC) AND THEN CHECKS THE RESULTS. IT IS AN OMEGA TASK THAT IS EXECUTED AFTER THE PC TEST DURING PREFLIGHT. IT IS THE LAST PREFLIGHT TEST AND IT SEQUENCES TO THE SYNCHRONIZATION PROCESS.



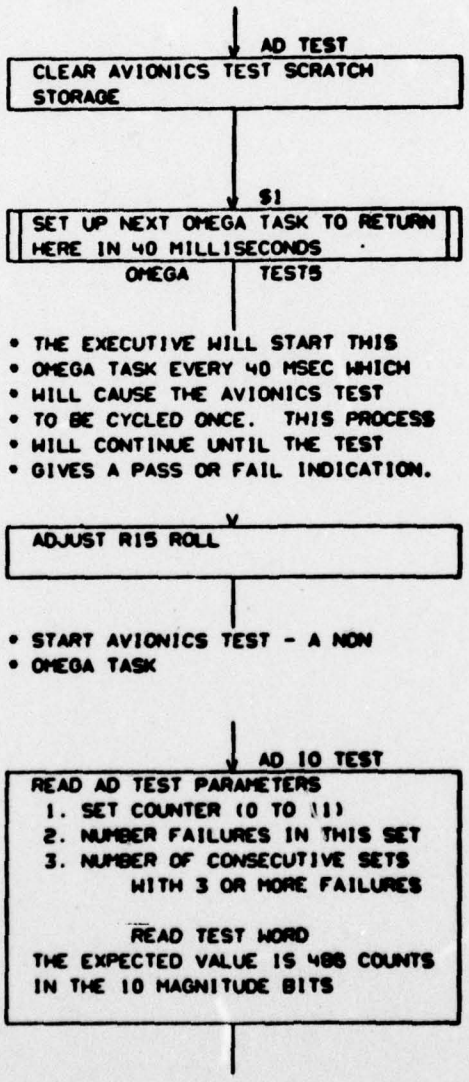
DMA TEST IS COMPLETE NOW
RESULTS ARE IN THE DMA
TEST LOCATION

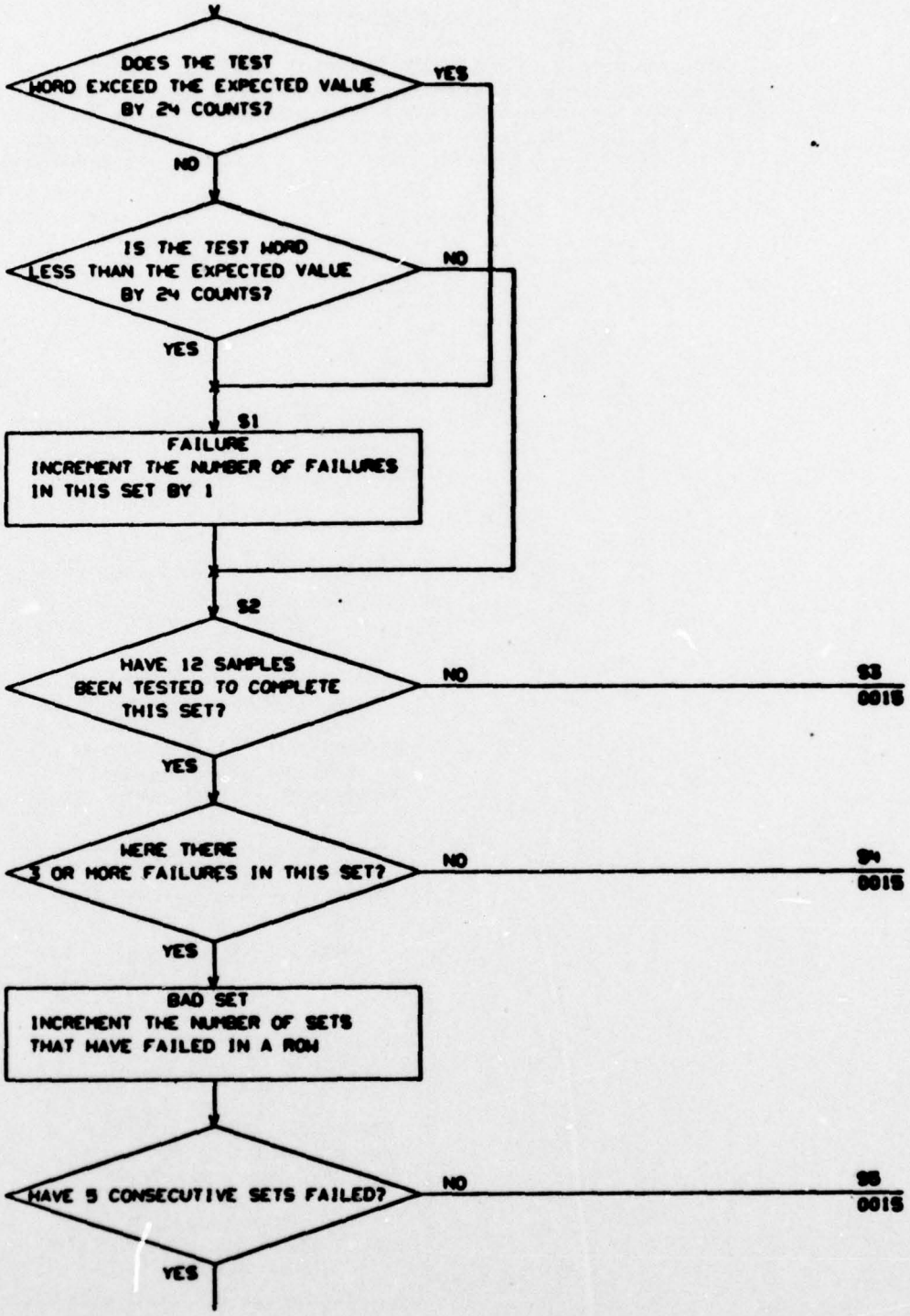


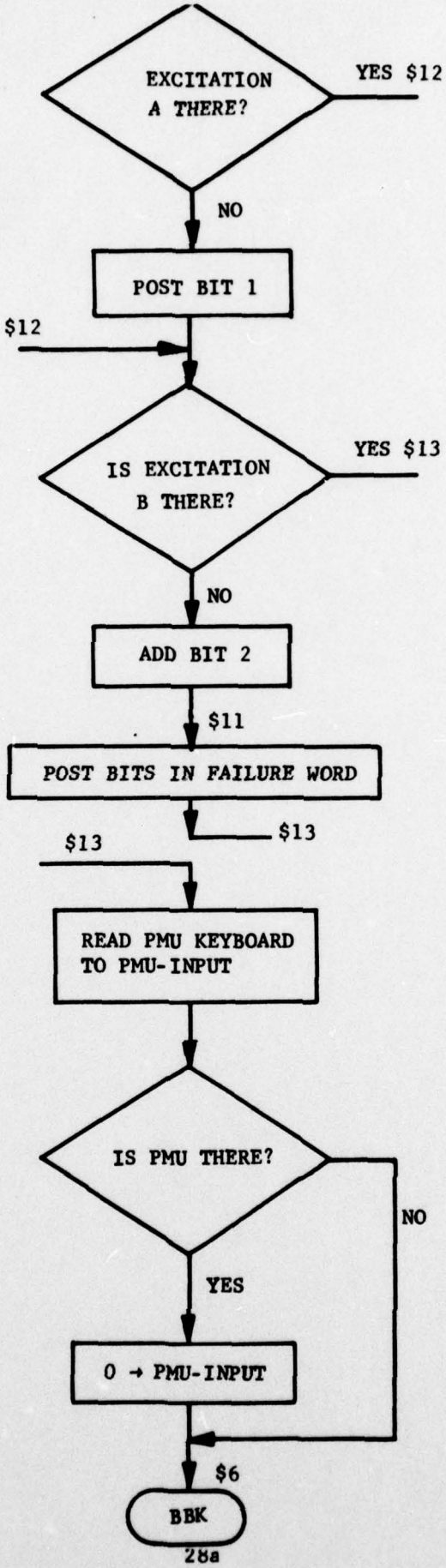

S2
TURN OFF ALL TEST SELECT BITS
IN THE TEST SELECT OUTPUT WORD
SIGNAL
EXIT - NEXT TASK IS SYNC
BBK

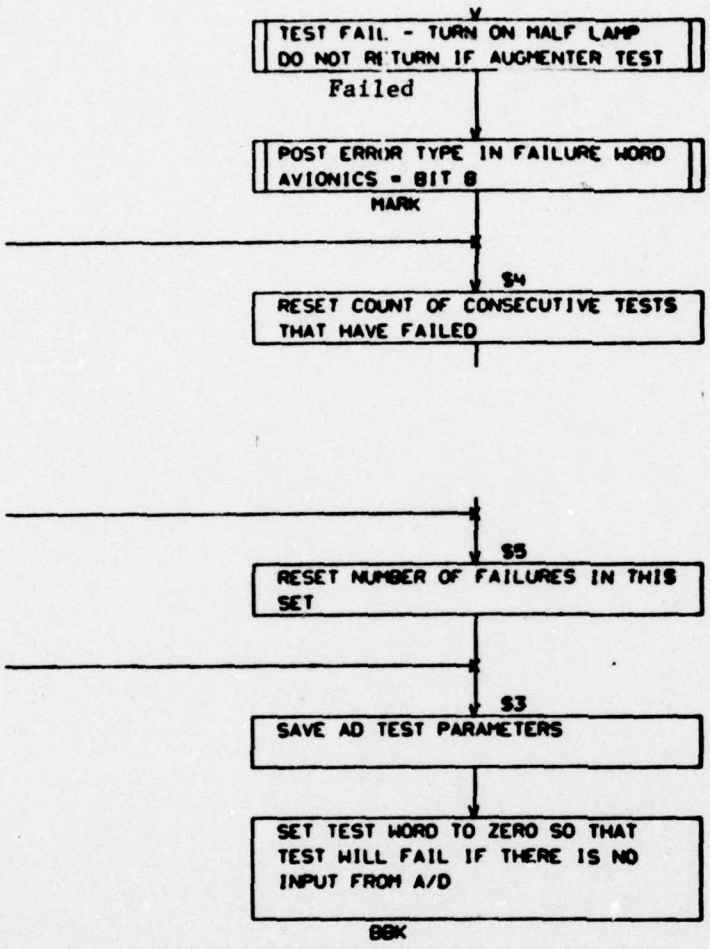
AVIONICS TEST

• THIS TEST IS EXECUTED EVERY .1 SECOND DURING SYSTEM OPERATION.
• IT EXAMINES THE A/D TEST WORD AND INDICATES A FAILURE WHEN IT
• IS OUT OF LIMITS AN EXCESSIVE NUMBER OF TIMES. THE TEST IS
• DIVIDED UP INTO SETS OF 12 SAMPLES. A FAILURE CONSISTS OF 3
• OR MORE BAD READINGS IN 5 CONSECUTIVE SETS.



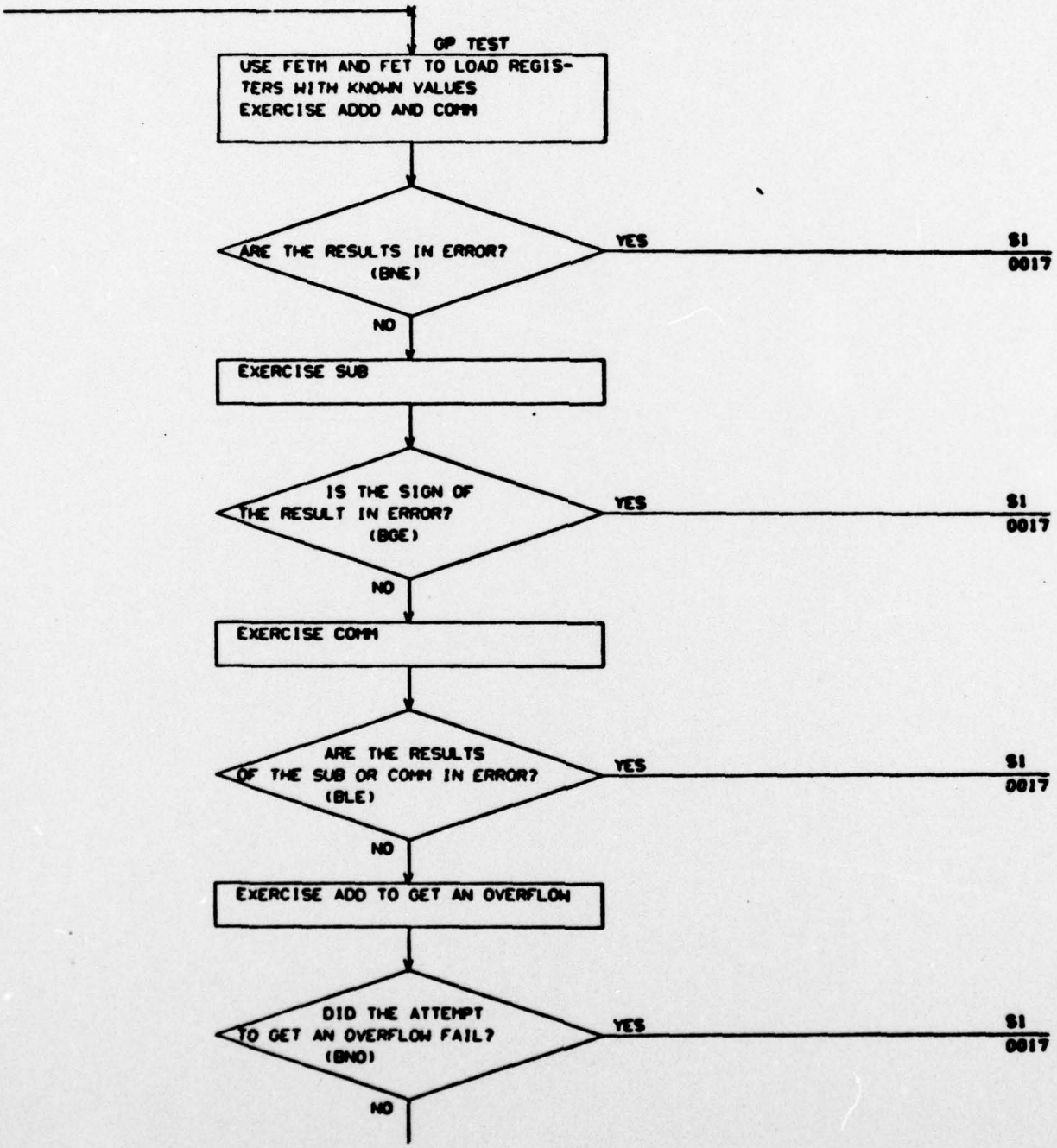

DOES THE TEST WORD EXCEED THE EXPECTED VALUE BY 24 COUNTS?
YES
NO
IS THE TEST WORD LESS THAN THE EXPECTED VALUE BY 24 COUNTS?
NO
YES
S1
FAILURE
INCREMENT THE NUMBER OF FAILURES IN THIS SET BY 1
S2
HAVE 12 SAMPLES BEEN TESTED TO COMPLETE THIS SET?
NO
S3
0015
YES
WERE THERE 3 OR MORE FAILURES IN THIS SET?
NO
S4
0015
YES
BAD SET
INCREMENT THE NUMBER OF SETS THAT HAVE FAILED IN A ROW
HAVE 5 CONSECUTIVE SETS FAILED?
NO
S5
0015
YES

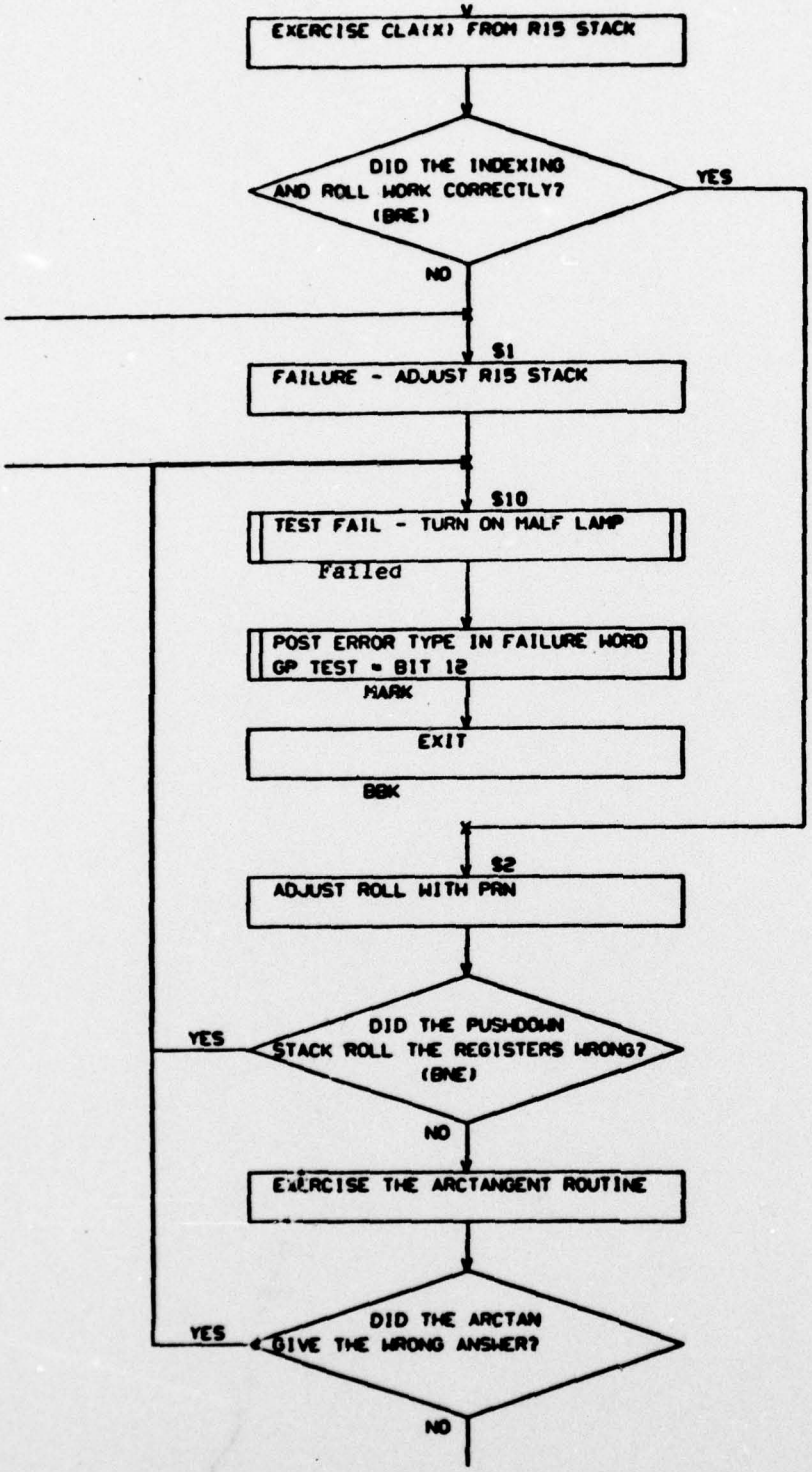

EXCITATION A THERE?
YES $12
NO
POST BIT 1
$12
IS EXCITATION B THERE?
YES $13
NO
ADD BIT 2
$11
POST BITS IN FAILURE WORD
$13
$13
READ PMU KEYBOARD TO PMU-INPUT
IS PMU THERE?
NO
YES
0 → PMU-INPUT
$6
BBK

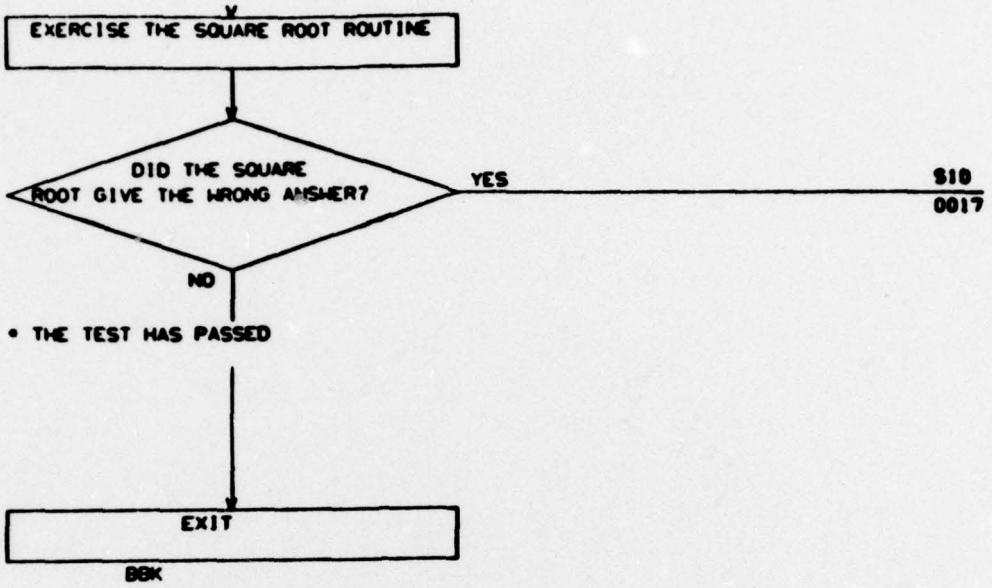

TEST FAIL - TURN ON MALF LAMP
DO NOT RETURN IF AUGMENTER TEST
Failed
POST ERROR TYPE IN FAILURE WORD
AVIONICS = BIT 8
MARK
$4
RESET COUNT OF CONSECUTIVE TESTS
THAT HAVE FAILED
$5
RESET NUMBER OF FAILURES IN THIS
SET
$3
SAVE AD TEST PARAMETERS
SET TEST WORD TO ZERO SO THAT
TEST WILL FAIL IF THERE IS NO
INPUT FROM A/D
BBK

1070 A/C TEST

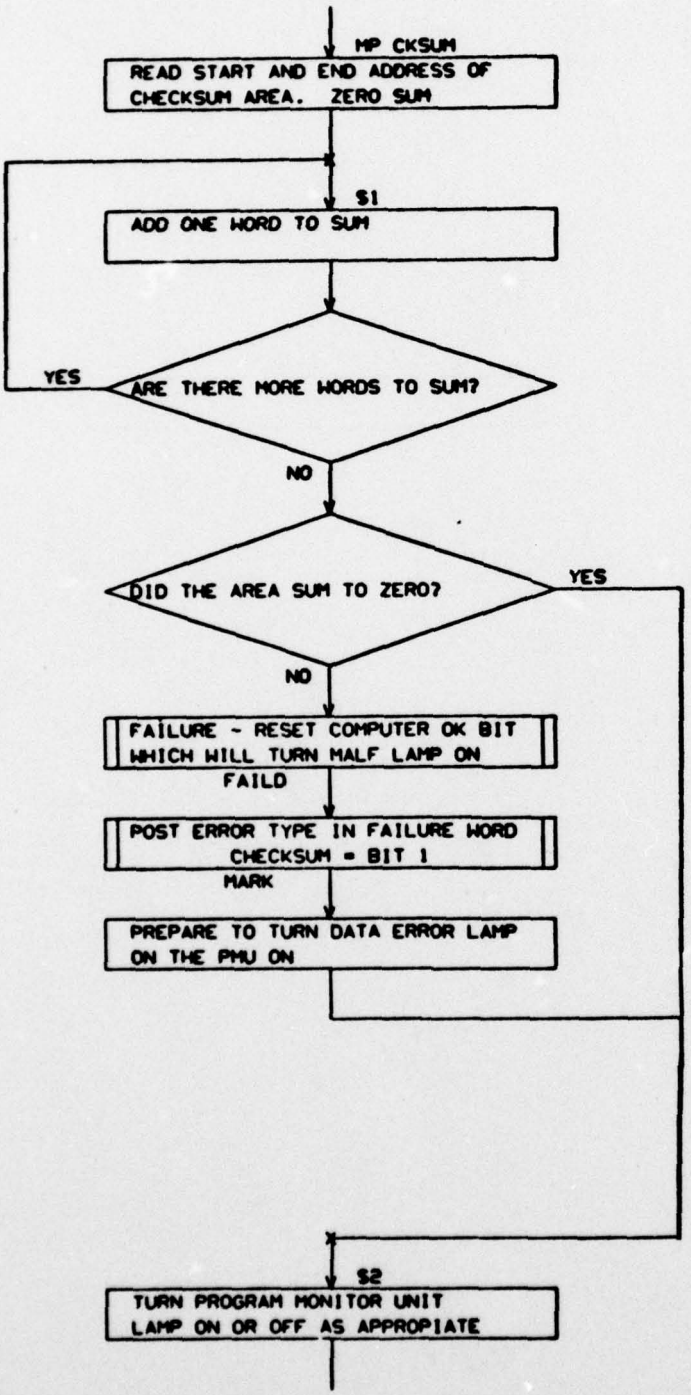
THIS TEST EXERCISES VARIOUS INSTRUCTIONS IN THE 1070 REPERTOIRE AND CHECKS THE RESULTS. IT IS A SLOW NON OMEGA TASK (ONCE PER SECOND)

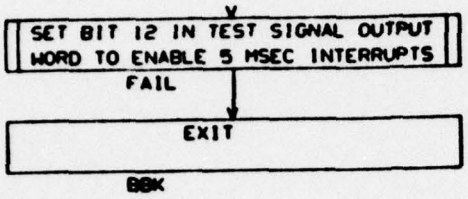



EXERCISE CLA(X) FROM R15 STACK
DID THE INDEXING AND ROLL WORK CORRECTLY? (BRE)
YES
NO
$1
FAILURE - ADJUST R15 STACK
$10
TEST FAIL - TURN ON MALF LAMP
Failed
POST ERROR TYPE IN FAILURE WORD GP TEST = BIT 12
MARK
EXIT
BBK
$2
ADJUST ROLL WITH PRN
DID THE PUSHDOWN STACK ROLL THE REGISTERS WRONG? (BNE)
YES
NO
EXERCISE THE ARCTANGENT ROUTINE
DID THE ARCTAN GIVE THE WRONG ANSWER?
YES
NO

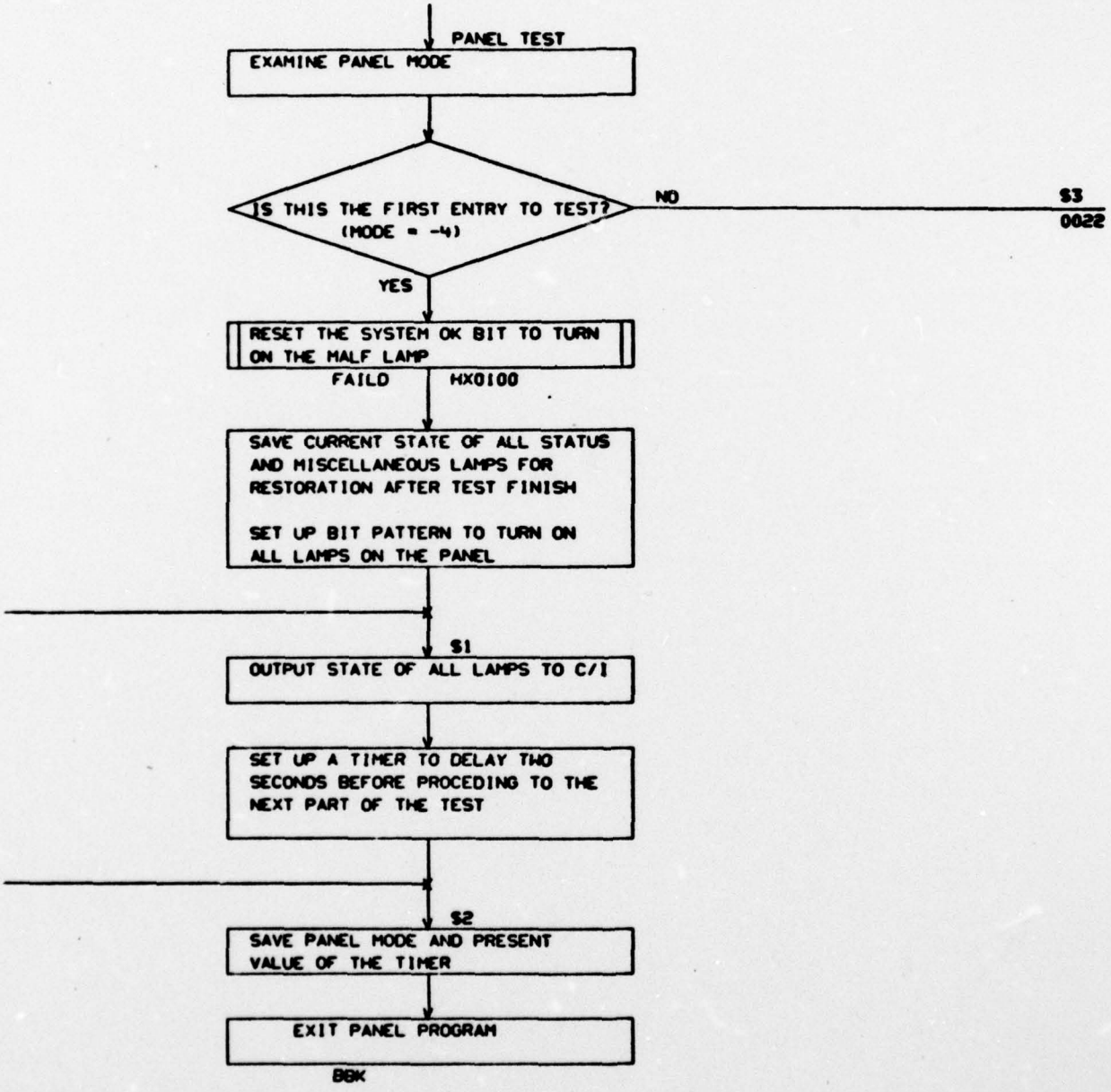

EXERCISE THE SQUARE ROOT ROUTINE
DID THE SQUARE ROOT GIVE THE WRONG ANSWER?
YES
$10
0017
NO
• THE TEST HAS PASSED
EXIT
BBK

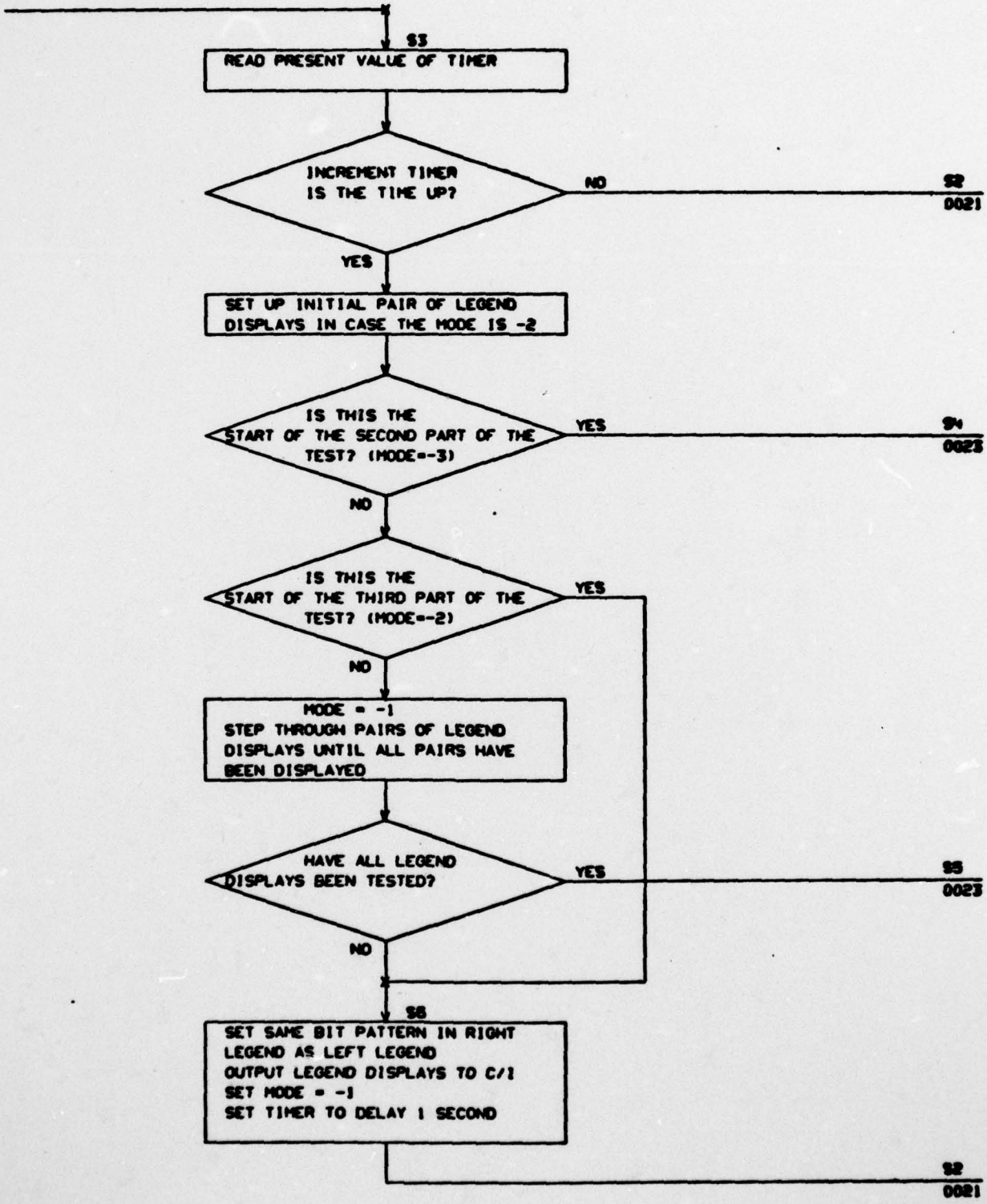
- MEMORY CHECKSUM - SUM ALL WORDS OF
- MEMORY EXCEPT VARIABLE STORAGE
- RESULT SHOULD BE ZERO

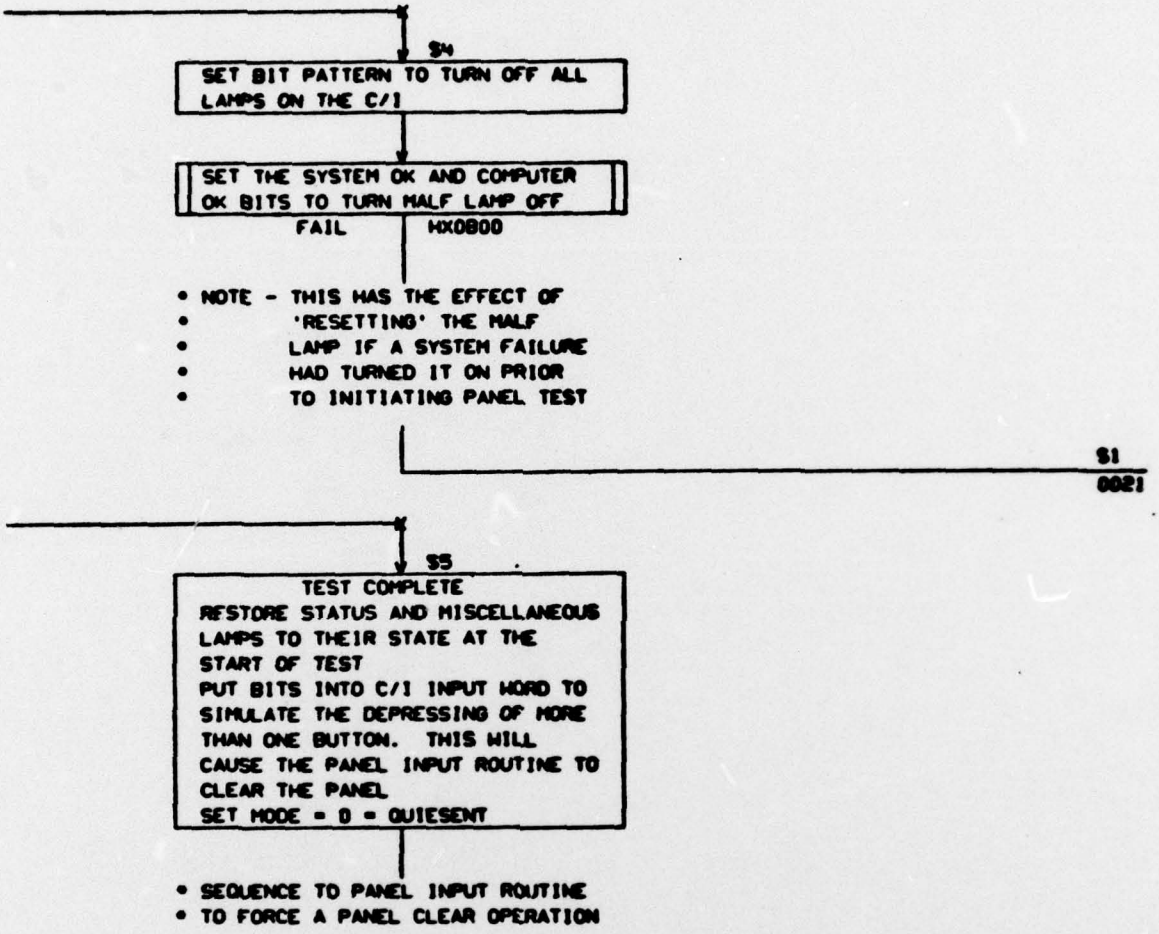



SET BIT 12 IN TEST SIGNAL OUTPUT
WORD TO ENABLE 5 MSEC INTERRUPTS
FAIL
EXIT
BBK

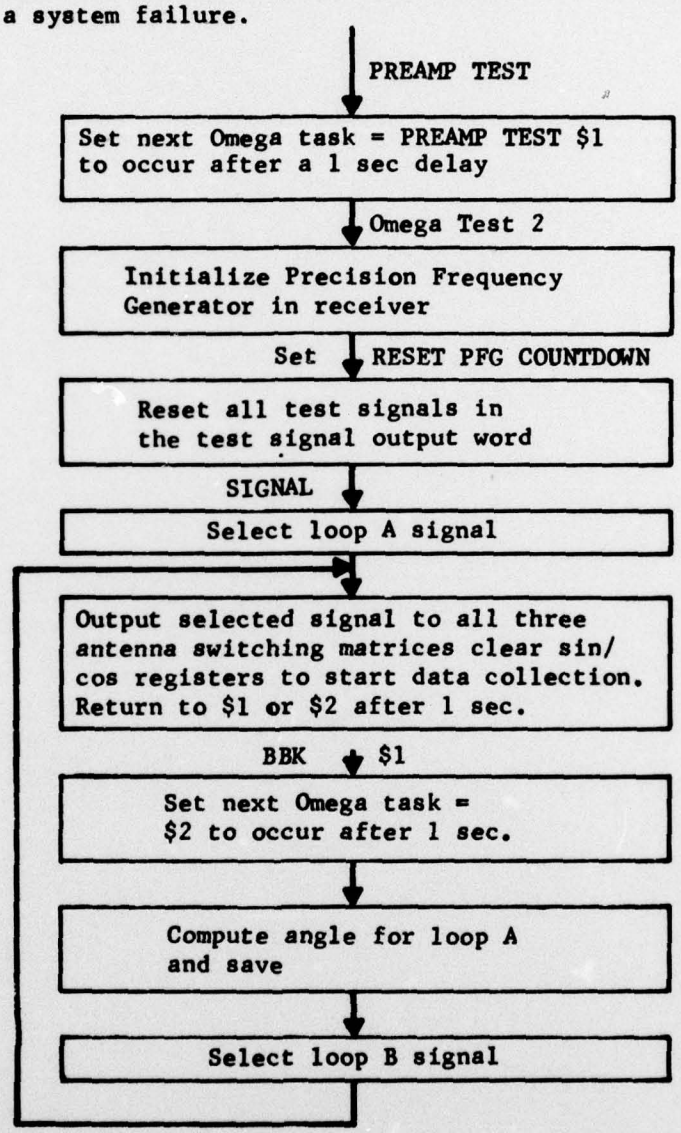
```
•                          PANEL TEST
•
• THIS PART OF THE C/I PROGRAM IS EXECUTED AFTER THE OPERATOR DEPRESSES
• THE PANEL TEST BUTTON.  IT CYCLES ALL OF THE LAMPS AND DISPLAYS ON THE
• PANEL IN 10 SECONDS.  IT ALSO TURNS OFF THE MALFUNCTION LAMP.
•
```

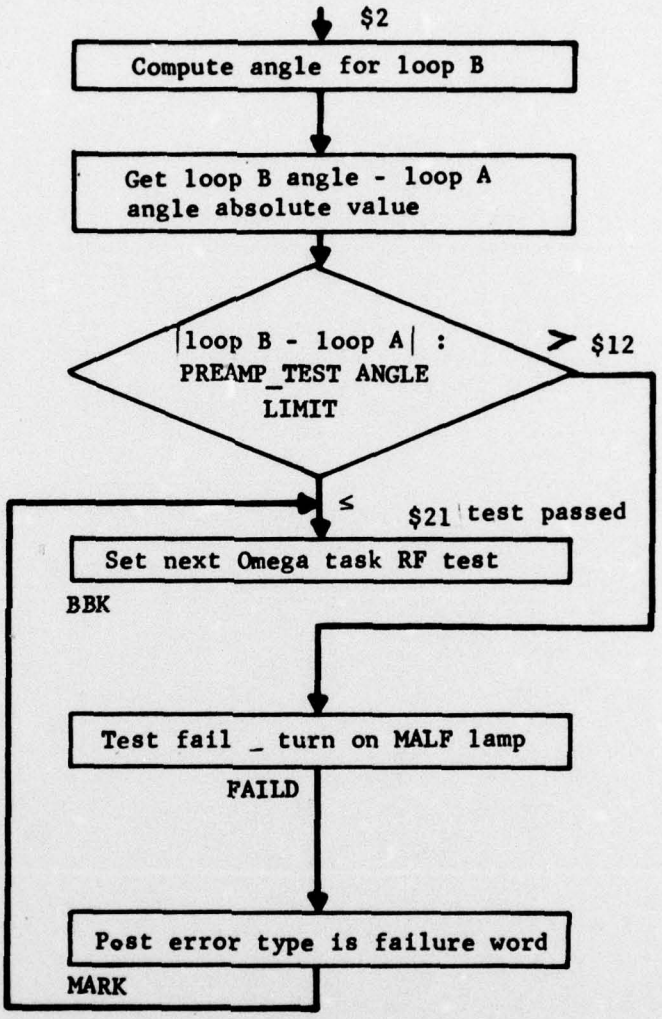


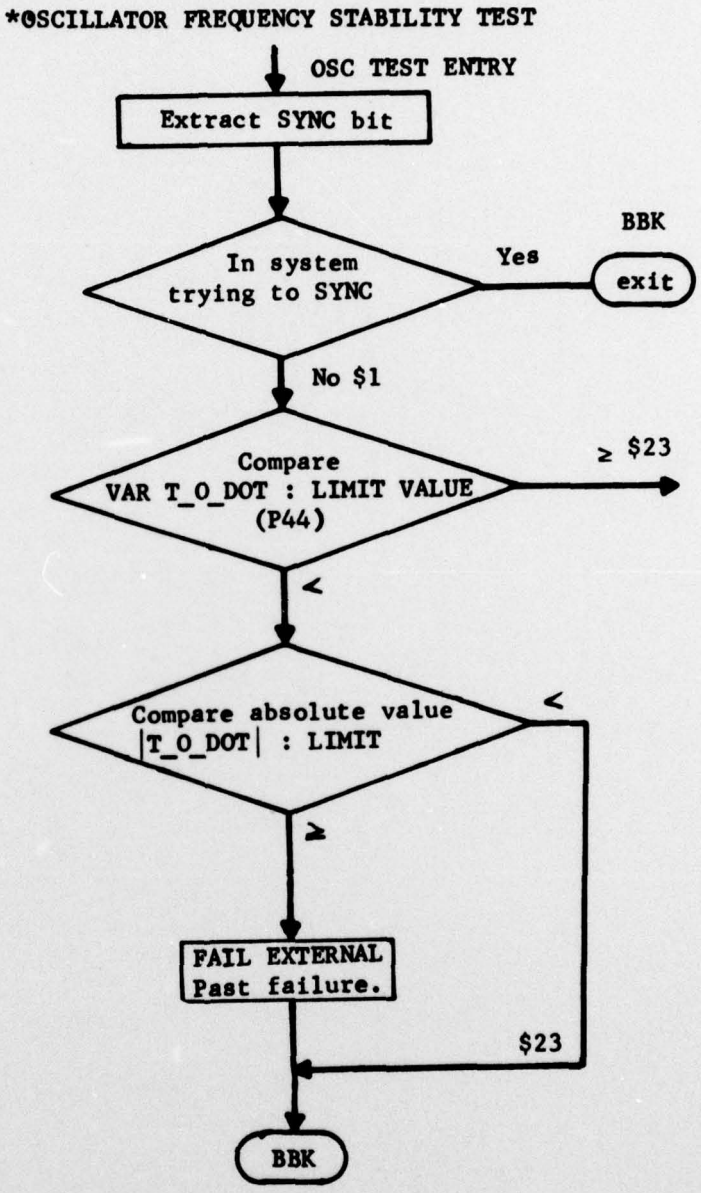

S3
READ PRESENT VALUE OF TIMER
INCREMENT TIMER
IS THE TIME UP?
NO
S2
0021
YES
SET UP INITIAL PAIR OF LEGEND
DISPLAYS IN CASE THE MODE IS -2
IS THIS THE
START OF THE SECOND PART OF THE
TEST? (MODE=-3)
YES
S4
0023
NO
IS THIS THE
START OF THE THIRD PART OF THE
TEST? (MODE=-2)
YES
NO
MODE = -1
STEP THROUGH PAIRS OF LEGEND
DISPLAYS UNTIL ALL PAIRS HAVE
BEEN DISPLAYED
HAVE ALL LEGEND
DISPLAYS BEEN TESTED?
YES
S5
0023
NO
S6
SET SAME BIT PATTERN IN RIGHT
LEGEND AS LEFT LEGEND
OUTPUT LEGEND DISPLAYS TO C/I
SET MODE = -1
SET TIMER TO DELAY 1 SECOND
S2
0021


$4
SET BIT PATTERN TO TURN OFF ALL LAMPS ON THE C/I
SET THE SYSTEM OK AND COMPUTER OK BITS TO TURN MALF LAMP OFF
FAIL
HX0800
• NOTE - THIS HAS THE EFFECT OF
• 'RESETTING' THE MALF
• LAMP IF A SYSTEM FAILURE
• HAD TURNED IT ON PRIOR
• TO INITIATING PANEL TEST
$1
0021
$5
TEST COMPLETE
RESTORE STATUS AND MISCELLANEOUS LAMPS TO THEIR STATE AT THE START OF TEST
PUT BITS INTO C/I INPUT WORD TO SIMULATE THE DEPRESSING OF MORE THAN ONE BUTTON. THIS WILL CAUSE THE PANEL INPUT ROUTINE TO CLEAR THE PANEL
SET MODE = 0 = QUIESENT
• SEQUENCE TO PANEL INPUT ROUTINE
• TO FORCE A PANEL CLEAR OPERATION

```
* PREAMP TEST
* This test commands test signals derived from the Precision
* Frequency Generator (PFG) and couples them into the input of
* the two loop amplifiers in the interface box.  The computer
* then reads the receiver phase angle and compared this value a
* against a prestored value.  Any out-of-tolerance condition is
* defined as a system failure.
```




$2
Compute angle for loop B
Get loop B angle - loop A angle absolute value
|loop B - loop A| : PREAMP_TEST ANGLE LIMIT
> $12
≤
$21 test passed
Set next Omega task RF test
BBK
Test fail _ turn on MALF lamp
FAILD
Post error type is failure word
MARK


*OSCILLATOR FREQUENCY STABILITY TEST
OSC TEST ENTRY
Extract SYNC bit
In system trying to SYNC
Yes
BBK
exit
No $1
Compare VAR T_O_DOT : LIMIT VALUE (P44)
≥ $23
<
Compare absolute value |T_O_DOT| : LIMIT
<
≥
FAIL EXTERNAL Past failure.
$23
BBK

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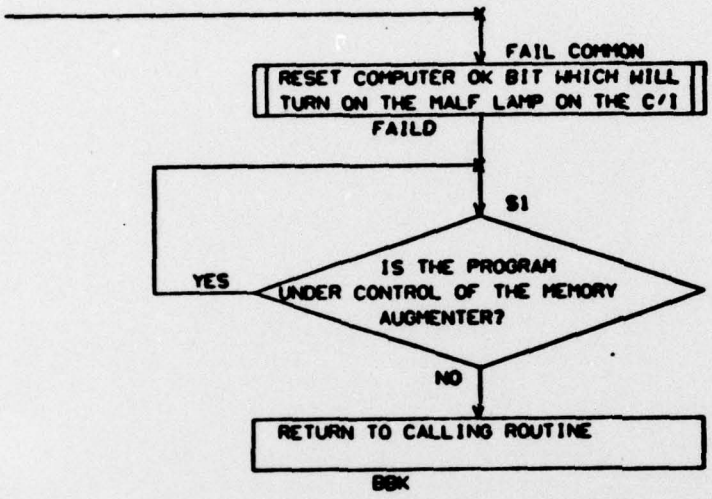
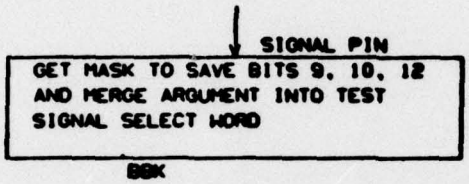
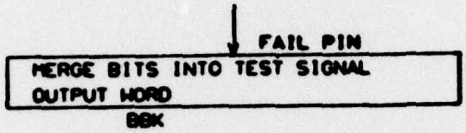
```
•     FAIL COMMON
•
•
• THIS ROUTINE WILL TURN ON THE
• MALF LAMP AND RETURN IF SYSTEM
• TEST.  IF THE AUGMENTER IS IN
• CONTROL THE PROGRAM WILL DELAY
• UNTIL THE AUGMENTER STOPS THE
• COMPUTER.
•
```



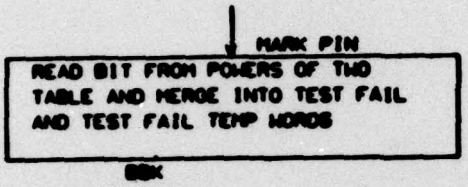
```
•     SIGNAL PIN
•
•
• THIS ROUTINE WILL MERGE THE
• SINGLE ARGUMENT INTO THE TEST
• SIGNAL SELECT WORD WITHOUT
• DISTURBING THE INTERRUPT INHI-
• BIT OR SYSTEM OR COMPUTER OK
• BITS (12, 10 AND 9)
•
```



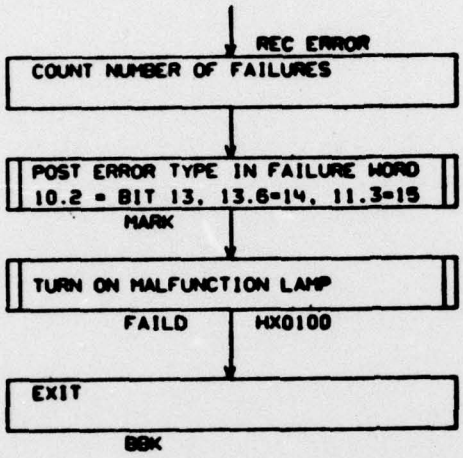
```
•              FAIL
•
• THIS PIN ROUTINE POSTS BITS IN THE
• TEST SIGNAL OUTPUT WORD. THE BITS ARE
• IN R0 AND THE MASK IS IN R1
```

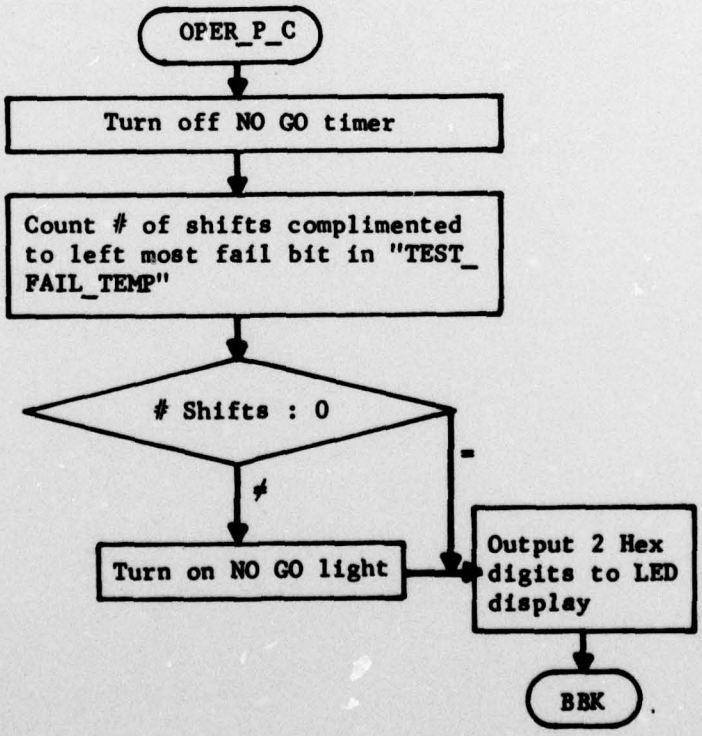


```
•
•
•              MARK
•
• THIS PIN ROUTINE WILL SET BITS IN A TEST
• FAIL WORD GIVEN THE BIT NUMBER IN R0
```



```
•          RECEIVER ERROR
•
• THIS ROUTINE IS ENTERED WHENEVER
• THE BIAS OR SCALE FACTOR ARE OUT
• OF LIMITS.
```





3.3 COMPUTER SUBPROGRAM ENVIRONMENT

3.3.1 Test Temporary Storage

The test routines use six of the twelve words available in the scratch storage called BEARING TEMPS. All other temporary storage used by the test routine is in the R15 pushdown stack.

3.3.2 Input/Output Formats

a) Antenna Select: DMA words 20_{16}, 21_{16}, and 22_{16} control the antenna and calibrate signals that are routed into the 10.2 kHz, 13.6 kHz receivers respectively. Table 1 gives the bit position, mnemonic and function for each signal. These words are accessed once every five (5) milliseconds.

TABLE 1 ANTENNA SELECT OUTPUT SIGNAL FORMAT

Bit	Mnemonic	Function
1	R(X)A	Antenna Loop A
2	R(X)AQ	Antenna Loop A - 90° (OMNI)
3	R(X)B	Antenna Loop B
4	R(X)AB	Antenna Loop - B
5	R(X)TQ	Calibrate/Test (inverted)
6	R(X)T	Calibrate/Test
7	I C(X)	Inverse
8-16	--	Unused

A separate discrete signal is available that will tell the program if an OMNI antenna is available to the system.

b) Test: DMA word 23_{16} controls the selection of system tests plus other miscellaneous signals that have previously been discussed. Table 2 defines the significance of each bit of the word. The word is accessed by the special I/O once every 5 milliseconds.

TABLE 2 OUTPUT TEST AND MISCELLANEOUS SIGNALS WORD

Bit	Function
1	PRE AMP Test (EETSA)
2	Not Used
3	Phase Angle to Digital Converter Test
4	Phase Counter I/O Test
5	Not Used
6	Not Used
7	Not Used
8	Not Used
9	Receiver/Computer No-Go
10	System Malfunction
11	Antenna Coupler Malfunction Indicator
12	Allow Special I/O Interrupts
13	Input/Output - DMA Test
14	Not Used
15	Not Used
16	Not Used

The Receiver-Computer NO-GO signal will be posted if the program detects a system problem that can be isolated to the Receiver-Computer. This will turn on a lamp on the Receiver-Computer box that must be manually reset. As long as this lamp is on the SYSTEM lamp on the C & I Panel will be illuminated. The System Malfunction bit will be posted by the program any time a system malfunction is detected. The SYSTEM lamp on the C & I Panel will also be illuminated when this signal is given. In addition, the SYSTEM lamp will be illuminated if the hardware detects a failure in the basic computer clock or if the Program Monitor signal is not given every 80 milliseconds by the program.

3.3.3 Required System Library Subroutines

Subroutine	Flow Diagram	Subprogram Design Document (by Vol. Number)
ATAN	P3/$4 P3/$4+1 P17/$2+2	XII
OMEGA	P1/1 P11/DMA TEST P4/2 P11/$1 P5/1 P13/$1 P9/PC TEST P9/$1	IX
SQRT	P18/1	XII

TABLE 3 FAILURE MODE DISPLAY

FAIL WORD MNEMONIC = TEST_FAIL_TEMP

	MEMORY LOCATION 002F		MEMORY LOCATION 002E	
BIT POSITION →	16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1		16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1	
Failure Description	Panel Display	PC LED Display		
Oscillator T_0	AUTO	F4		
Excitation A	9	F3		
Excitation B	8	F2		
RF Pre-Amp	7	F1		
RCUR 11.3 kHz	6	F0		
RCUR 13.6 kHz	5	EF		
RCUR 10.2 kHz	4	EE		
G.P. Test	3	ED		
DMA I/O	2	EC		
Phase Counter Down	1	EB		
Phase Counter Up	0	EA		
Avionics I/O	G	E9		
Phase/Digital 11.3 kHz	F	E8		
VLF 11.3 kHz	E	E7		
Phase/Digital 13.6 kHz	D	E6		
VLF 13.6 kHz	C	E5		
Phase/Digital 10.2 kHz	B	E4		
VLF 10.2 kHz	A	E3		
Checksum	S	E2		